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Benchmarking of EUV lithography line/space patterning versus immersion lithography multipatterning schemes at equivalent pitch

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ABSTRACT

In this paper, the authors compare and contrast the line/space patterning performance of direct print EUV to multipatterning schemes at equivalent pitch using a systematic unbiased PSD analysis approach for the 7nm and 5nm logic node critical BEOL layers. The authors highlight where innovation is needed to move forward with EUV in terms of line edge roughness (LER), line width roughness (LWR) performance.

Keywords: EUV direct print, multipatterning, LER, LWR, SWR, line/space patterning.

1. INTRODUCTION

EUV implementation into high volume manufacturing is set to take place in the second or third iteration of the 7nm node foundry logic for contacts and vias (see Figure 1). In contrast, industry experts forecast line-space EUV patterning for the back end of line (BEOL) will be delayed and might not be implemented until late 7nm or even 5nm node [1].

Multipatterning has enabled continuous scaling of CMOS technology in both the front end of line (FEOL) and the back end of line (BEOL). However, moving from multipatterning to direct print (single patterning) EUV for BEOL 1X metal presents several advantages. Not only can the number of masks and exposures be reduced from three immersion prints (one SAQP + two cuts) down to one EUV print, concerns of edge placement error of the blocks in regards to the grid are completely eliminated as the blocks and lines are printed at once. In addition, electrical characteristics of EUV direct print patterns have shown tighter distributions than their multipatterning counterparts and better pattern fidelity [2]. Some of the downsides of EUV printed patterns are line edge roughness (LER) and line width roughness (LWR), which have shown to degrade BEOL dielectric reliability performance [3],[4], if the low frequency roughness cannot be controlled to within 8-10% of the critical dimension of the line.

Beyond 7nm node, EUV multipatterning will be required to follow the latest IRDS roadmap (Figure 2), which calls for aggressive metal pitch scaling in the BEOL as well as transistor structure evolution from Finfet to lateral nanowires and vertical nanowires. Few comparative studies of multipatterning schemes versus EUV for advanced technology nodes have been conducted previously [5]. In an effort to assess EUV patterning performance readiness from a roughness perspective we conduct a systematic power spectral density analysis of the unbiased LER/ LWR for various multipatterning schemes and contrast these results to equivalent pitch EUV printed patterns. This analysis is performed for both the first generation of EUV implementation at the 7nm node and the second generation of EUV patterning targeting the 5nm node. While the benefits of spacer-based pitch splitting approaches are well known (the ALD spacer conformality provides correlated edges leading to a very low linewidth variation), variability, pitch walking control all resulting in edge placement error can be an issue and can be remediated by EUV direct print implementation provided the LER/LWR can meet the demanding targets of advanced logic nodes.

Finally, we will look forward to the 3nm node early patterning performance by combining EUV lithography with a spacer-based pitch splitting approach and assess the challenges of going beyond direct print.

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7nm Foundry logic			7nm Foundry logic 2nd Gen			7nm Foundry logic 3rd Gen			5nm Foundry logic		
Layer	Pitch (nm)	Lithography	Layer	Pitch (nm)	Lithography	Layer	Pitch (nm)	Lithography	Layer	Pitch (nm)	Lithography
Fin	29-30	SAQP	Fin	29-30	SAQP	Fin	29-30	SAQP	Fin	20	SAQP
Gate	56-57	SADP	Gate	56-57	SADP	Gate	56-57	SADP	Gate	45-50	SADP
Contact	~56-57	LE3	Contact	~56-57	EUV	Contact	~56-57	EUV	Contact	45-50	EUV
1x Metal	40 1D	SADP	1x Metal	40 1D	SADP	1x Metal	36 2D	EUV	1x Metal	26 1D	EUV
1x Via	~60	LE3	1x Via	~60	EUV	1x Via	~60	EUV	1x Via	38	EUV

2018 | Early 2019 | Late 2019 | 2020

Source: IC Knowledge Scotten Jones

Figure 1: EUV Lithography insertion forecast for foundry technology based on IC Knowledge [1].

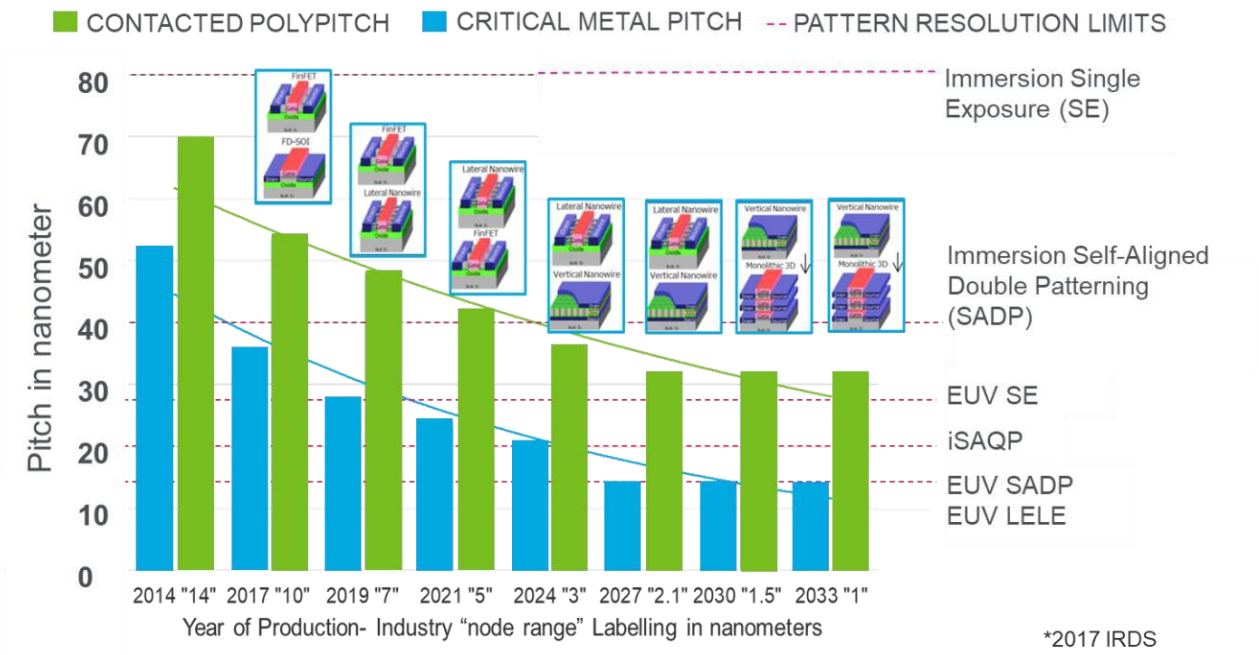


Figure 2: Scaling and scaling forecast from IRDS roadmap 2017 for metal pitch and gate pitch with patterning resolution limits overlapped on figure.

2. UNBIASED ROUGHNESS MEASUREMENT METHODOLOGY

The following review of the measurement of roughness follows the discussion found in reference [6]. Rough features are most commonly characterized by the standard deviation of the edge position (for LER), linewidth (for LWR), and feature centerline for pattern placement roughness (PPR). The standard deviation describes a variation in a direction perpendicular to an edge, but characteristics of this deviation along the length of the line is important as well. The line-length dependence is most commonly assessed using the power spectral density (PSD), as seen in Figure 3. The low-frequency region, corresponding to long length scales, is typically flat indicating a white noise behavior which is characterized by its extrapolated zero-frequency value, PSD(0). The turn towards lower PSD values at higher frequencies (short length scales) is caused by correlations in the roughness along the line length. The correlation length defines this turning point length. Figure 4 shows two

PSDs from two edges with the same variance (the same area under the PSD curve) but with different values of PSD(0) and correlation length.

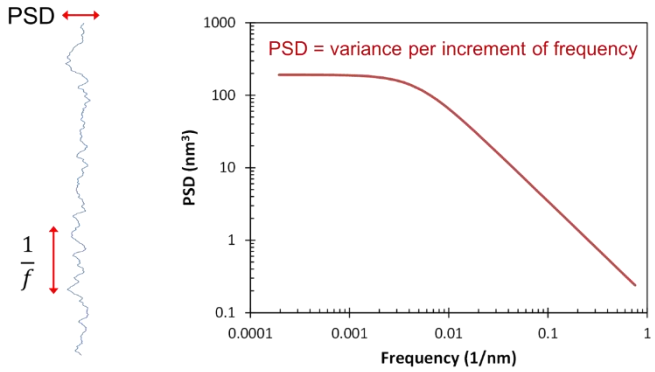


Figure 3: An example of a rough edge and its corresponding power spectral density (PSD). From Ref. 6.

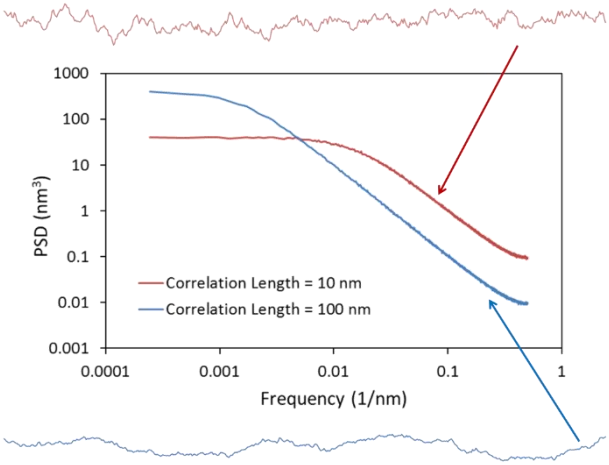


Figure 4: Two edges can have very different PSD behavior even though the standard deviations of the roughness are the same. From Ref.6.

By far the most common way to measure feature roughness is the top-down CD-SEM (critical dimension scanning electron microscope). The biggest impediment to accurate roughness measurement is noise in the CD-SEM image. SEM images suffer from shot noise, where the number of electrons detected for a given pixel varies randomly. For the expected Poisson-like distribution, the variance in the number of electrons detected for a given pixel of the image is equal to the expected number of electrons detected for that pixel. Since the number of detected electrons is proportional to the number of electrons that impinge on that pixel, noise can be reduced by increasing the electron dose that the sample is subjected to. For many samples (especially photoresist), high electron dose leads to sample damage (resist line slimming, for example). Thus, to prevent sample damage electron dose is kept as low as possible, where the lowest dose possible is limited by the noise in the resulting image. Figure 5 shows portions of three SEM images of nominally the same lithographic features taken at different electron doses.

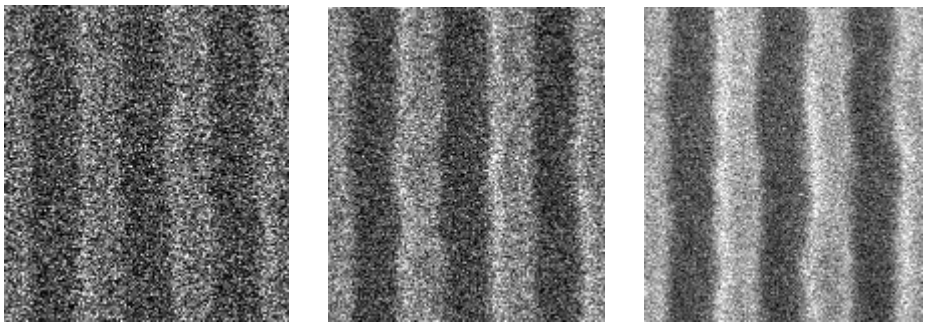


Figure 5: Portions of SEM images of nominally identical resist features with 2, 8, and 32 frames of integration (respectively, from left to right). Doubling the frames of integration doubles the electron dose per pixel. Since the dose is increased by a factor

SEM image noise adds to the actual roughness of the patterns on the wafer to produce a measured roughness that is biased higher.[6]

$$\sigma^2_{biased} = \sigma^2_{unbiased} + \sigma^2_{noise} \quad (1)$$

where σ_{biased} is the roughness measured directly from the SEM image, $\sigma_{unbiased}$ is the unbiased roughness (that is, the true roughness of the wafer features), and σ_{noise} is the random error in detected edge position (or linewidth) due to noise in the SEM imaging. Since an unbiased estimate of the feature roughness is obviously what is desired, the measured roughness must be corrected by subtracting an estimate of the noise term.

In a related issue, excessive image noise can reduce the robustness of edge detection. The solution to this problem is typically to filter the image, smoothing out the high frequency noise. Figure 6 shows an example of using a simple threshold edge detection algorithm with and without image filtering [7]. Without image filtering, the edge detection algorithm is mostly detecting the noise in the image and does not reliably find the edge. But the use of image filtering can have a large effect on the resulting PSD. Figure 7 shows the impact of two different image filters on the measured PSDs from a collection of 30 images [8]. Obviously, the high-frequency region is greatly affected by filtering. But even the low frequency region of the PSD shows a noticeable change when using a smoothing filter. As will be described next, the use of image filtering makes measurement and subtraction of image noise impossible.

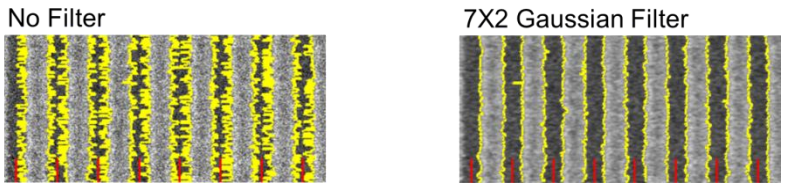


Figure 6: Detecting edges in a noisy SEM image with and without the use of an image filter. From Ref. 8.

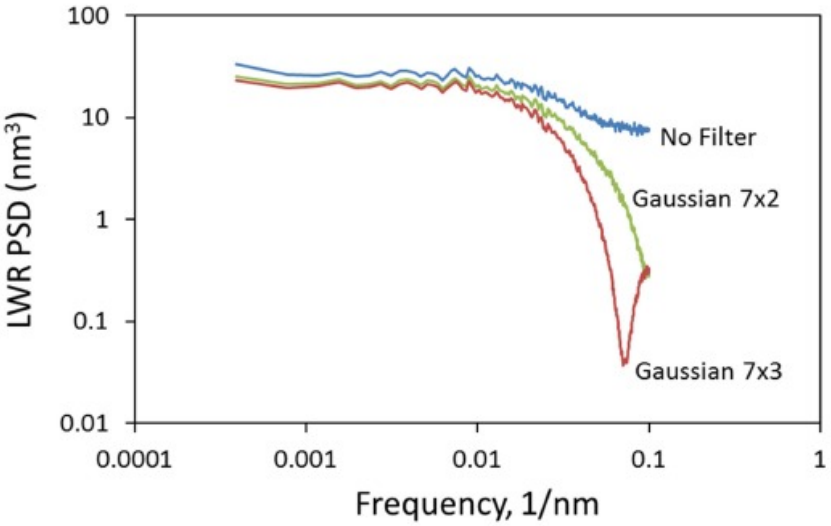


Figure 7: Power spectral densities from many rough features with images preprocessed using a 7x2 or 7x3 Gaussian filter, or not filtered at all. From Ref. 8.

If edge detection without image filtering can be accomplished, noise measurement and subtraction can be achieved by contrasting the PSD behavior of the noise with the PSD behavior of the actual wafer features. We expect resist features (as well as after-etch features) to have a PSD behavior as shown in Figure 1. Correlations reduce high-frequency roughness so that the roughness becomes very small over very small length scales. SEM image noise, on the other hand, can be reasonably assumed to be white noise, so that the noise PSD is flat. Thus, at a high enough frequency the measured PSD will be dominated by image noise and not actual feature roughness (the so-called "noise floor") [9]. Thus, measurement of the high-frequency PSD (in the absence of any image filtering) provides a measurement of the SEM image noise. Figure 8 illustrates this approach. Clearly, this approach to noise subtraction cannot be used on PSDs coming from images that have been filtered since the filtering removes the high-frequency noise floor (see Figure 7).

The key to using the above approach of SEM noise subtraction for obtaining an unbiased PSD is to robustly detect edges without the use of image filtering. This can be accomplished using an inverse linescan model [8] A linescan model predicts the SEM image linescan given a set of beam conditions and the feature geometry on the wafer. Ideally, such a model would be physically based, easily calibrated, and not computationally intensive. An inverse linescan model runs this linescan model in reverse: given a measured linescan, what wafer feature edge positions produce a linescan that best fits the data? Such an inverse linescan model can use the physics of SEM image formation to constrain the possible linescan shapes and reject the noise in the measured linescan to extract its signal. The Fractilia inverse linescan model was used to generate the no-filter PSD data shown in Figure 7 and will be used in the measurement of unbiased PSDs and roughness throughout the rest of this paper.

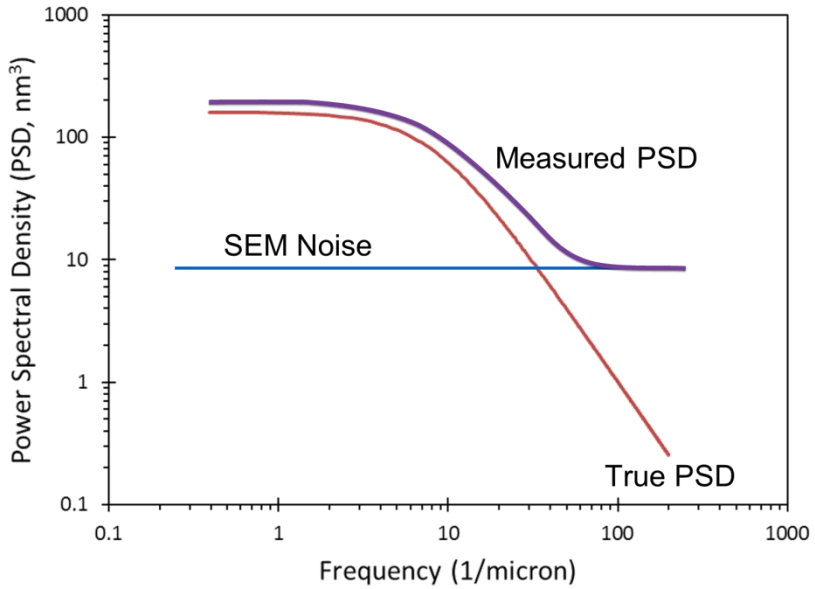


Figure 8: The principle of noise subtraction: using the power spectral density, measure the flat noise floor in the high-frequency portion of the measured PSD, then subtract this white SEM noise to get the true PSD. From Ref. 6.

3. MULTIPATTERNING TECHNIQUE ROUGHNESS EVOLUTION

3.1 SADP for BEOL hard mask open 40nm pitch line/space

3.1.1 Stack and flow description

The smallest pitch reachable using 193 immersion lithography being 80nm, one can achieve 40nm pitch by doubling the pattern density. For this flow, a tri-layer stack of one planarizing carbon layer, one silicone-based anti-reflective layer and photoresist is used to pattern a non-organic layer that will be used as a mandrel. After the mandrel is defined using dry etch, an atomic layer deposited dielectric film is used to form two sets of spacers on each side of the mandrel. The spacers are then used as a mask to transfer the features into a metal hard mask layer. We performed a top-down CD-SEM inspection after each of the steps shown on Figure 9.

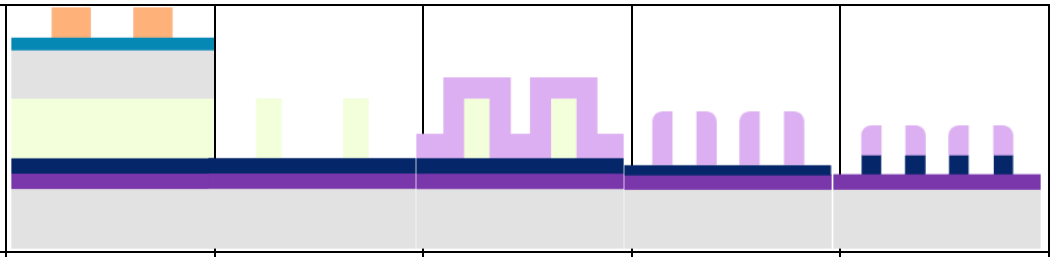
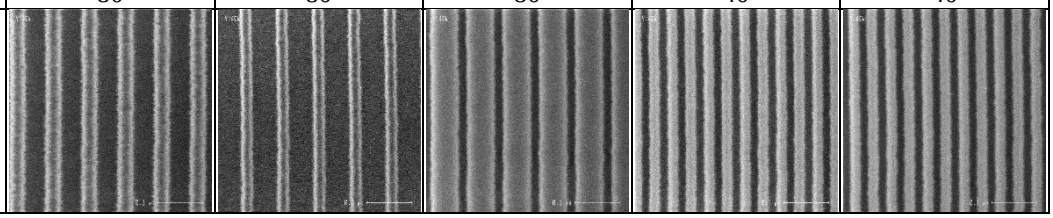
Stack illustration					
Patterning step	1- 193i lithography	2- Mandrel etch	3- ALD spacer	4- Spacer etch mandrel pull	5- Metal Hard Mask Open
Pitch (nm)	80	80	80	40	40
Rectangular top down (300k x49k) image					

Figure 9: Drawings and top down CD SEM evolution to form self-aligned double patterning (SADP) 40nm pitch.

3.1.2 Roughness evolution

Using rectangular scan images, we generated the following (Figure 10) unbiased PSD for both LER and LWR. Additionally, biased and unbiased 3-sigma values of the roughness were measured. On Figure 11, one can see the biased value as well as the unbiased value in which the noise has been subtracted.

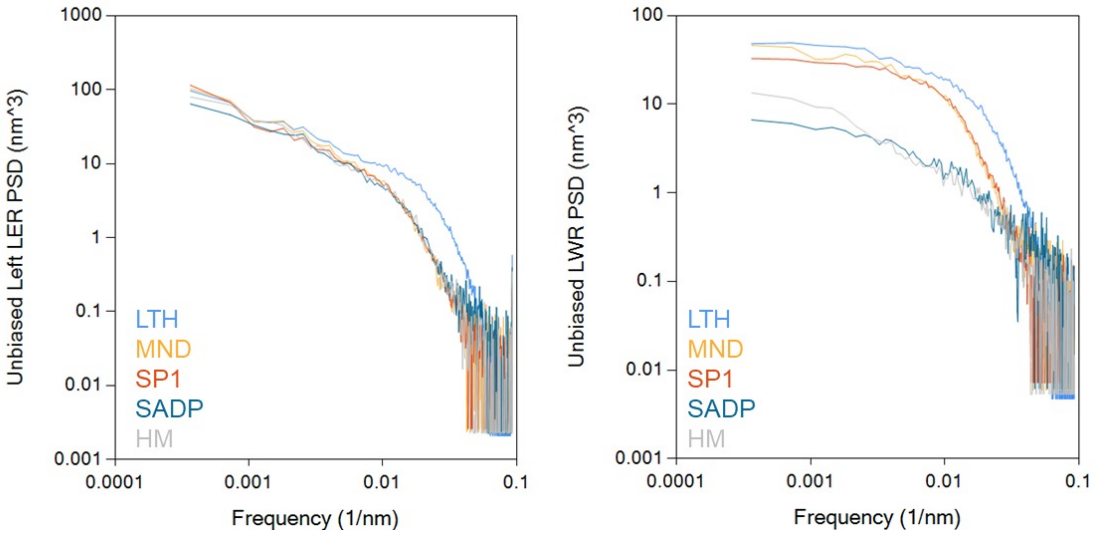


Figure 10: Unbiased PSD of Left-LER and LWR for each step used to form SADP 40nm pitch.

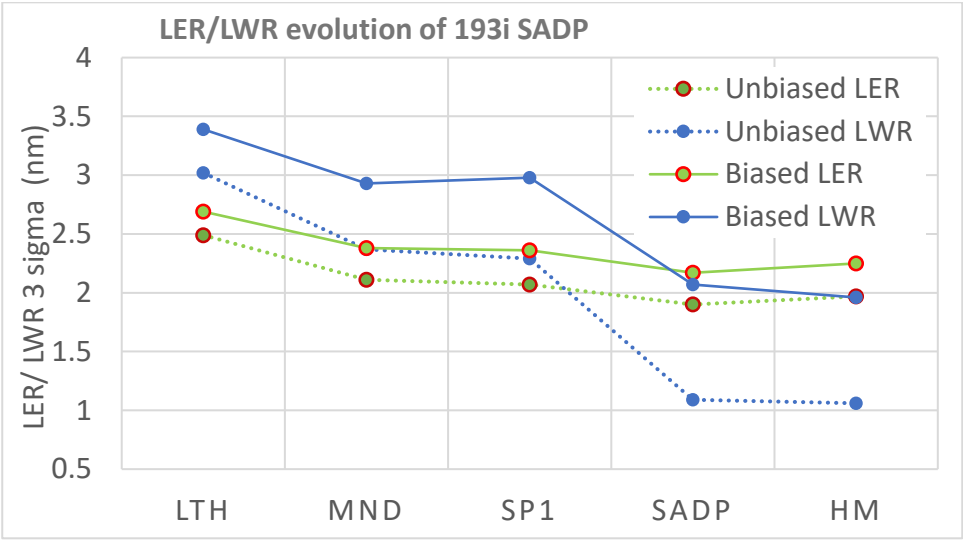


Figure 11: Biased and unbiased LER and LWR (3 sigma) value for each SADP steps.

The first thing one can observed is that while both unbiased and biased values are following the same trend, biased-unbiased differences ranges from 7% to 12% for LER and from 11 to 47% for LWR starting from lowest difference to highest at the end of the process. There is a significant LER drop from lithography at the first mandrel definition. This phenomenon is often observed with dry etch smoothing techniques [REF]. However after this step, the LER decrease during the subsequent steps is not as marked, which can be explain by the ALD conformality that will follow the roughness of the mandrel. It also means that no additional roughness is induced from the spacer etch-back/mandrel pull process. At the hard mask open step, we see a small uptick in LER average, which is driven by a low frequency increase as seen on Figure 10, while the LER at mid and high frequencies remains unaffected. Low frequency increase in LER is a sign of wiggling which is often driven either by aspect ratio or by stress and fundamental properties of films. Metal hard mask materials often contain significant stress and can cause wiggling post etch transfer, which seems to be the cause of that minor uptick based on the PSD shape and prior learning. For LWR, besides the reduction observed from lithography to mandrel definition, we see a drastic drop once the SADP patterns are formed. This is due to the spacers left and right edges correlation that are inherent of a self-aligned dual patterning techniques (see Figure 12).

While it is important to monitor the CD variation of the line (LWR) it is yet also important to look at the CD variation of the space, also called SWR for Space Width Roughness. In fact, the SWR will not follow the typical behavior of the LWR as its left and right side will not be correlated. For that reason, we also added unbiased SWR values to the step-by-step evolution (Figure 13) and one can see that the spacer CD variation remains stable once the pitch is split in half.

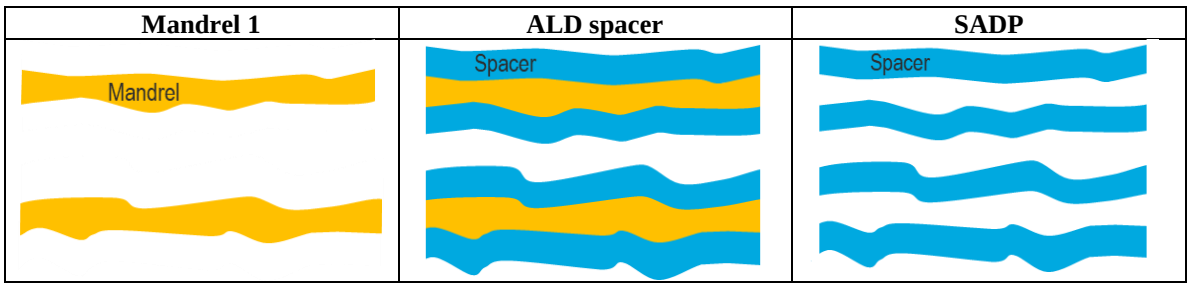


Figure 12: Illustration of SADP correlation of left and right spacer's edges.

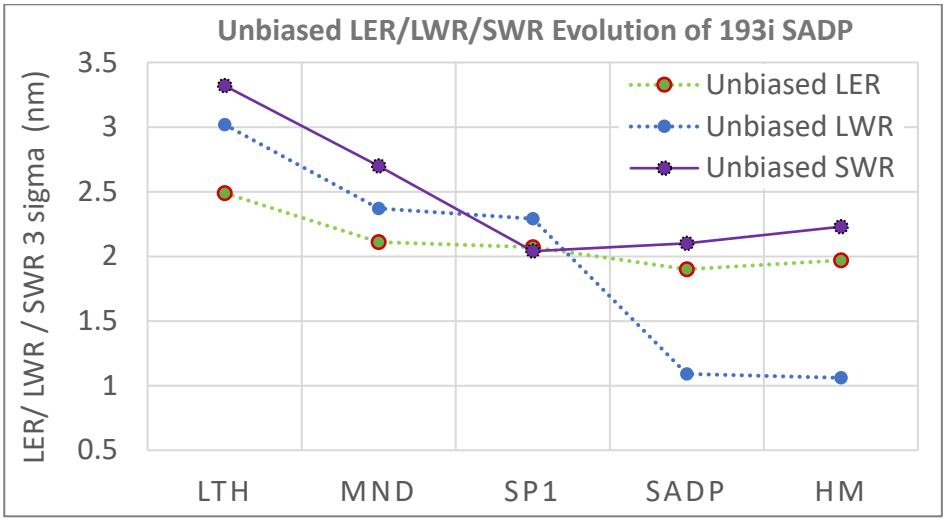


Figure 13: Unbiased SWR evolution of 193i SADP.

3.2 SAQP scheme targeting 30nm pitch line and space

3.2.1 Stack and flow description

To push 193i lithography even further, another possibility is to use the SADP technique twice, which is called self-aligned quadruple patterning or SAQP. To study the roughness evolution of this flow, we picked the following scheme (see Figure 14). The stack is made of (from top to bottom): photoresist on a silicone based anti-reflective layer, one planarizing carbon layer, one inorganic layer that will be used at a mandrel, one dielectric etch stop layer and one hard mask. The initial starting pitch from lithography is 120nm. The first pitch splitting occurs at the resist level through the steps 1, 2 and 3. Then the first sets of spacers formed are etched down into the tri-layer and the mandrel layer. At this point, a second ALD spacer is deposited and used to perform a spacer etch-mandrel pull that will reach the final pitch of 30nm. Finally these features are transferred into the target layer.

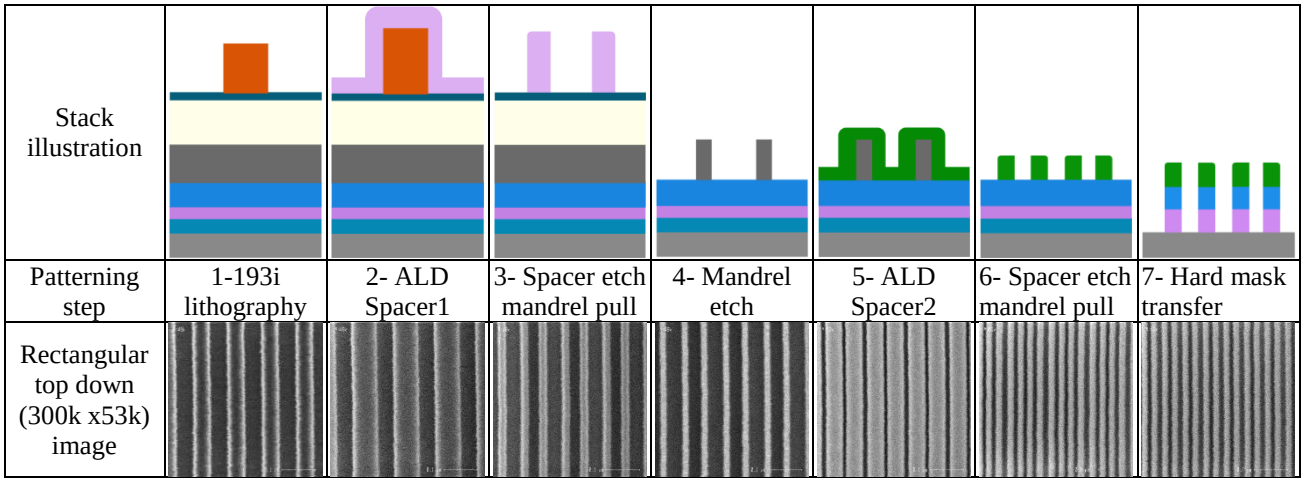


Figure 14: Drawings and top down CD SEM evolution to form SAQP at 30nm pitch.

3.2.2 Roughness analysis

With the same methodology, we generated the unbiased PSD of the Left-LER and LWR in Figure 15. The 3-sigma roughness values as shown in Figure 16. One can observe that again both biased and unbiased measurement are following the same trend. The biased vs unbiased values differences ranges from 9% to 24% for LER and 15 to 62% on LWR with the highest differences seen after SADP and SAQP steps.

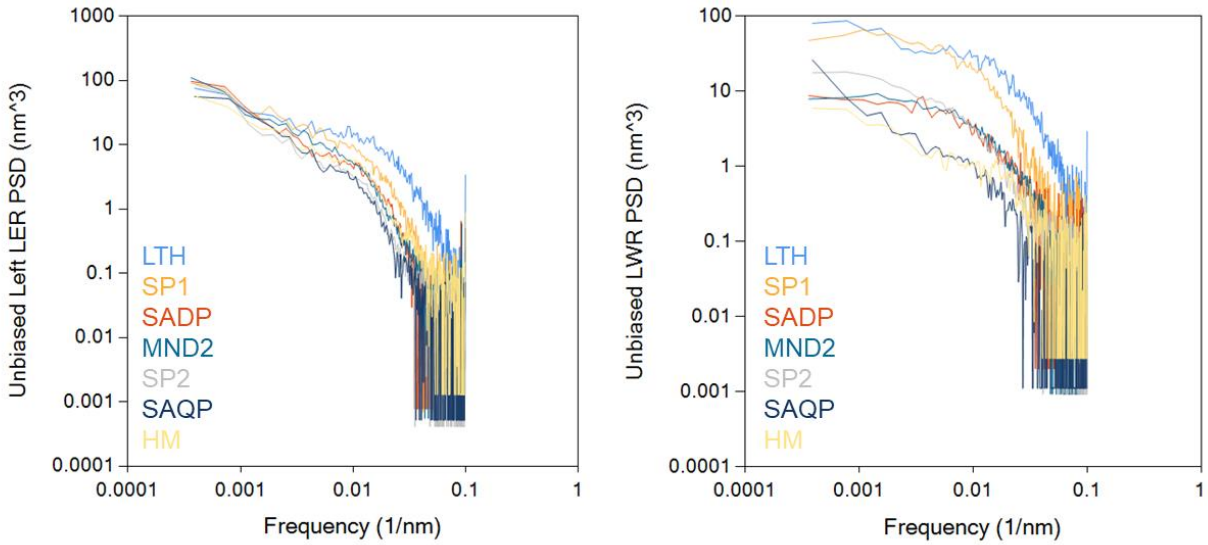


Figure 15: Unbiased PSD of Left-LER and LWR for each step used to form SAQP 30nm pitch.

Similar roughness behavior is observed through SADP steps. The LER is clearly improved from lithography to the first spacer deposition. It is further reduced once the first sets of spacers are formed. It is further reduced once the second sets of spacer are formed, then it remains constant until the last step. The LWR is also drastically reduced after SADP due to highly correlated edges from ALD spacer deposition. An additional LWR reduction is observed after SAQP which can be explained by an even further correlation of the edges. Now the SWR, a third important metric, shows a constant, almost linear reduction until the second spacer deposition. It then reaches a plateau until the final hard mask transfer step.

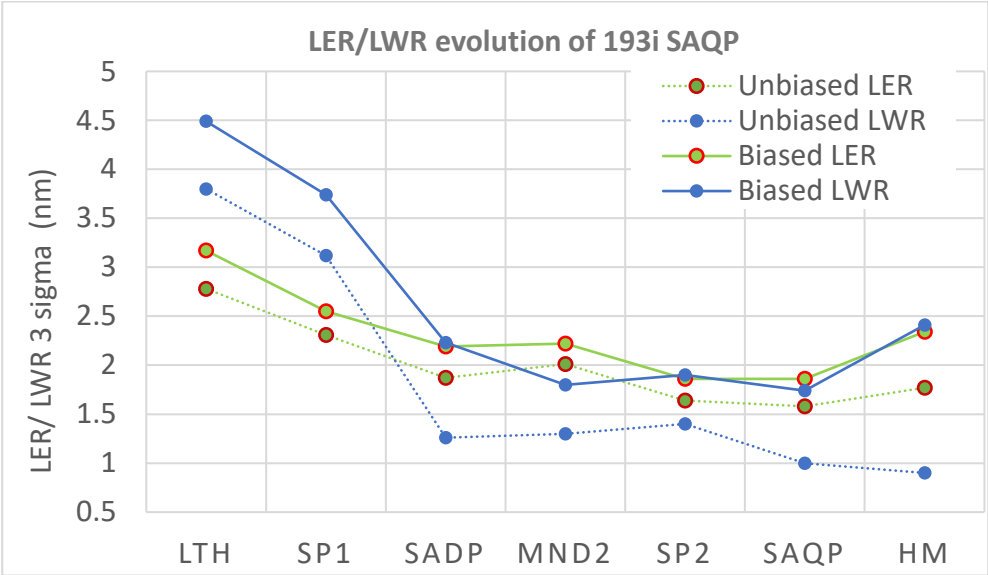


Figure 16: Biased and unbiased LER and LWR (3 sigma) value for each SAQP steps.

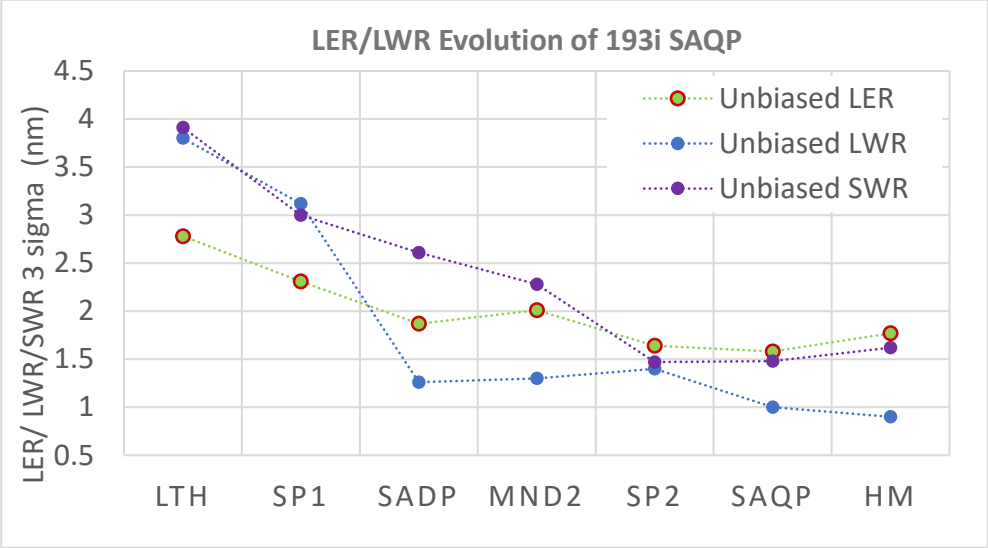


Figure 17: Unbiased SWR evolution of 193i SAQP.

Another relevant way to analyze the roughness performance of a scheme is to look at the percentage of the roughness relative to the CD. In this case we can see that the ratio of edge roughness increases with the pattern density to finally reach 10.5% after the final hard mask transfer. The percentage of LWR remains around 6% but the SWR also follows an almost linear increase until the SAQP patterns are formed, at which point the SWR represents about 12% of the space width. A more ideal case when forming SAQP would be to be able to keep the percentage of SWR the same across the steps. However, regarding the LER, as the line's CD is being divided by 4, if we assume no degradation nor reduction of the edge roughness from the initial mandrel, one can expect the percentage to follow a somewhat linear increase until it is multiplied by 4 after the SAQP lines are obtained.

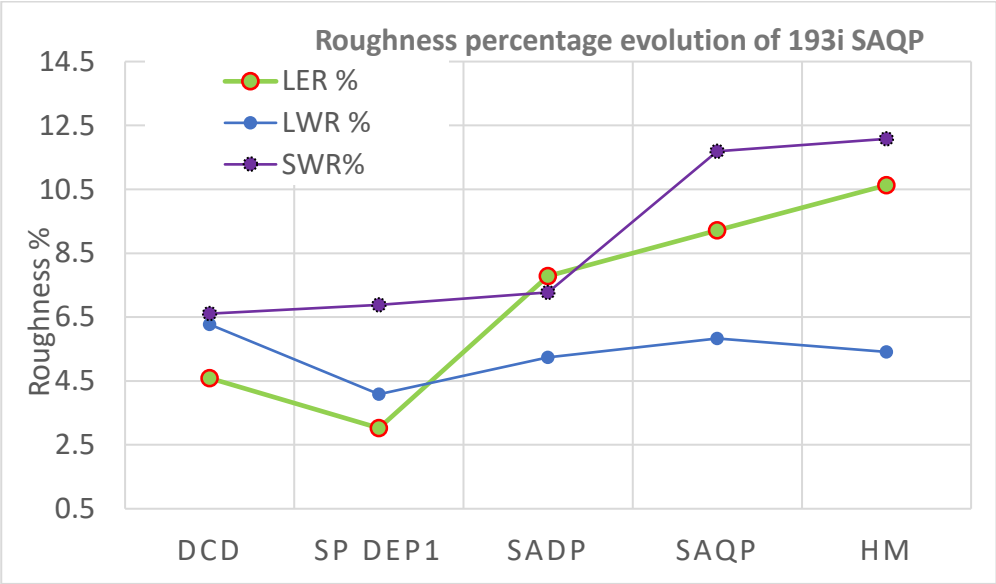


Figure 18: Percentage of unbiased roughness amount across SAQP steps.

3.3 SADP using first generation of EUV targeting 28nm line and space pitch

3.3.1 Stack and flow description

In this section, we describe an EUV SADP flow to reach 28nm final pitch. The stack and steps are described on Figure 19. With the exception of the type of lithography used, the layers used are very close to the 193i SADP scheme explained in the previous section.

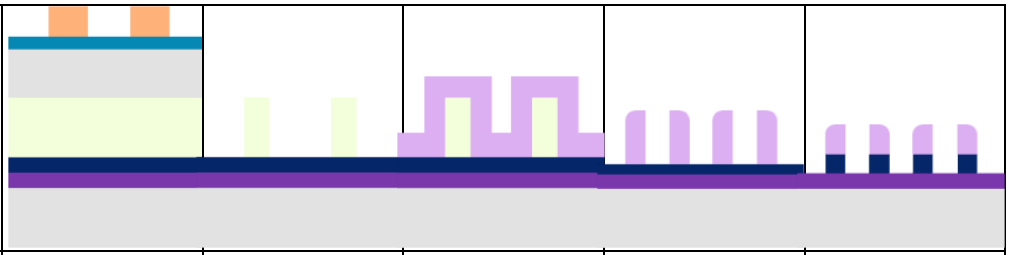
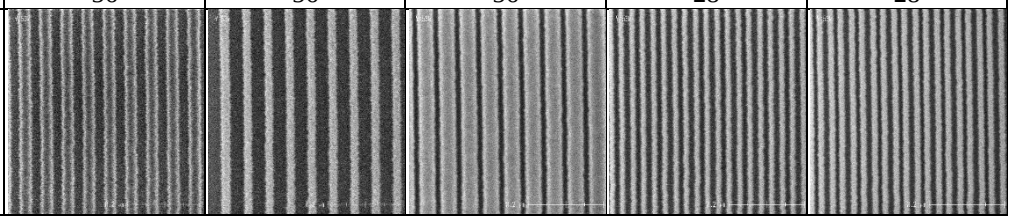
Stack illustration					
Patterning step	1- EUV lithography	2- Mandrel etch	3- ALD spacer	4- Spacer etch mandrel pull	5- Metal Hard Mask Open
Pitch (nm)	56	56	56	28	28
Rectangular top down (300k x53k) image					

Figure 19: Drawings and top down CD SEM evolution to form SADP 28nm pitch.

3.3.2 Roughness analysis

For this flow, we generated and compared biased and unbiased PSD of the LER and LWR, as shown in Figure 20. We then plotted the amount of roughness measured (Figure 21). This time the difference between the unbiased and the biased roughness varied from 14% to 23% for the LER and 19 to 70% for the LWR. The behavior of the roughness across the step is closely matched to the 193i SADP option seen in the previous section. As a result, the LWR plateau is reached after SADP and the LER also saturates after the ALD spacer is deposited.

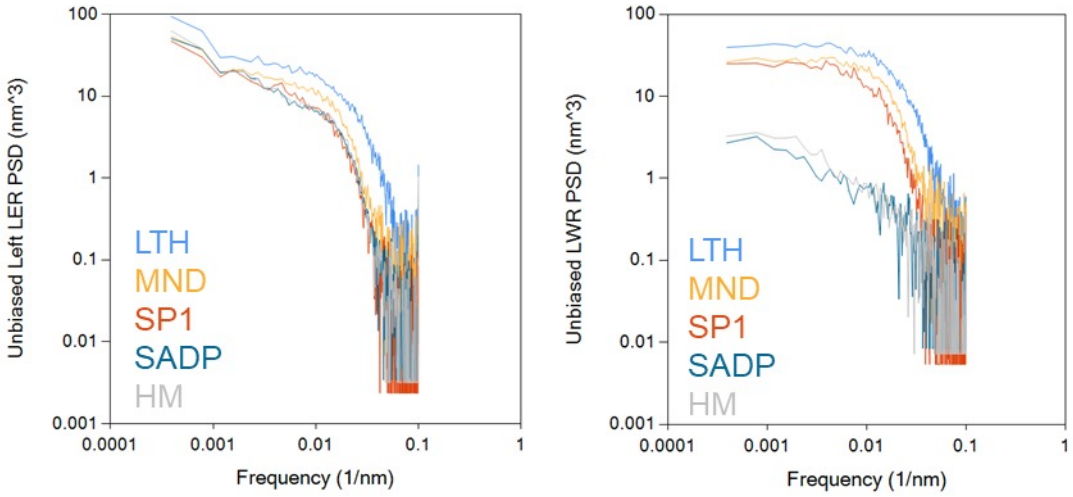


Figure 20: Unbiased PSD of Left-LER and LWR for each step used to form SADP 28nm pitch.

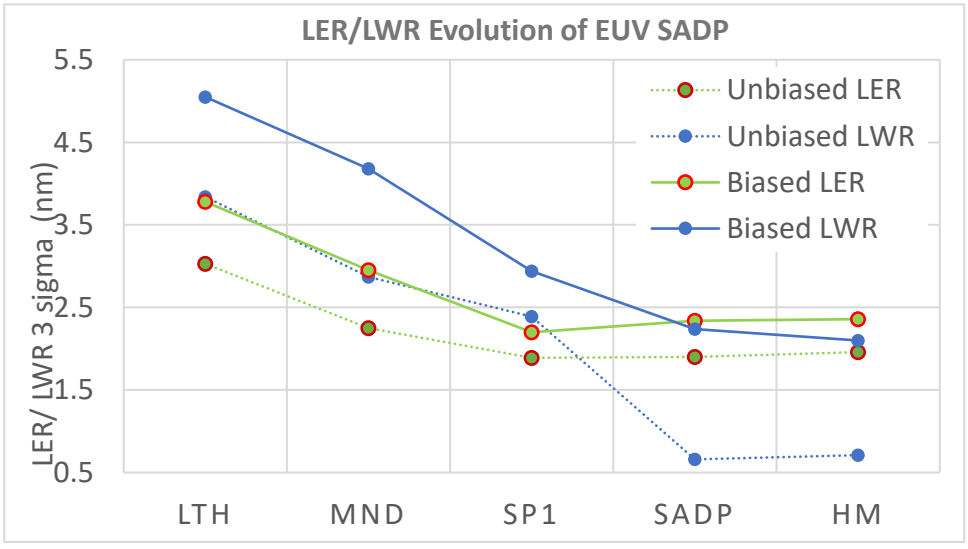


Figure 21: Biased and unbiased LER and LWR (3 sigma) value for each SADP steps.

4. EUV LITHOGRAPHY DIRECT PRINT ROUGHNESS ANALYSIS

4.1 EUV stacks for BEOL hard mask open

In this portion, we will focus on EUV lithography direct print, studying 40nm as well as 30nm pitch line and space. In both cases, a traditional Chemically Amplified Resist is used. Going from 40 to 30nm pitch required a drastic resist thickness reduction of around 40% in order to widen the lithography process window for pattern collapse [10]. In addition to this change and in order to further thin down the hard mask underlayer, a thin low temperature oxide hard mask is used under the organic adhesion layer. Adding the inorganic layer allows more flexibility in material choices and improved the defectivity. The main drawback is the increased process complexity and cost.

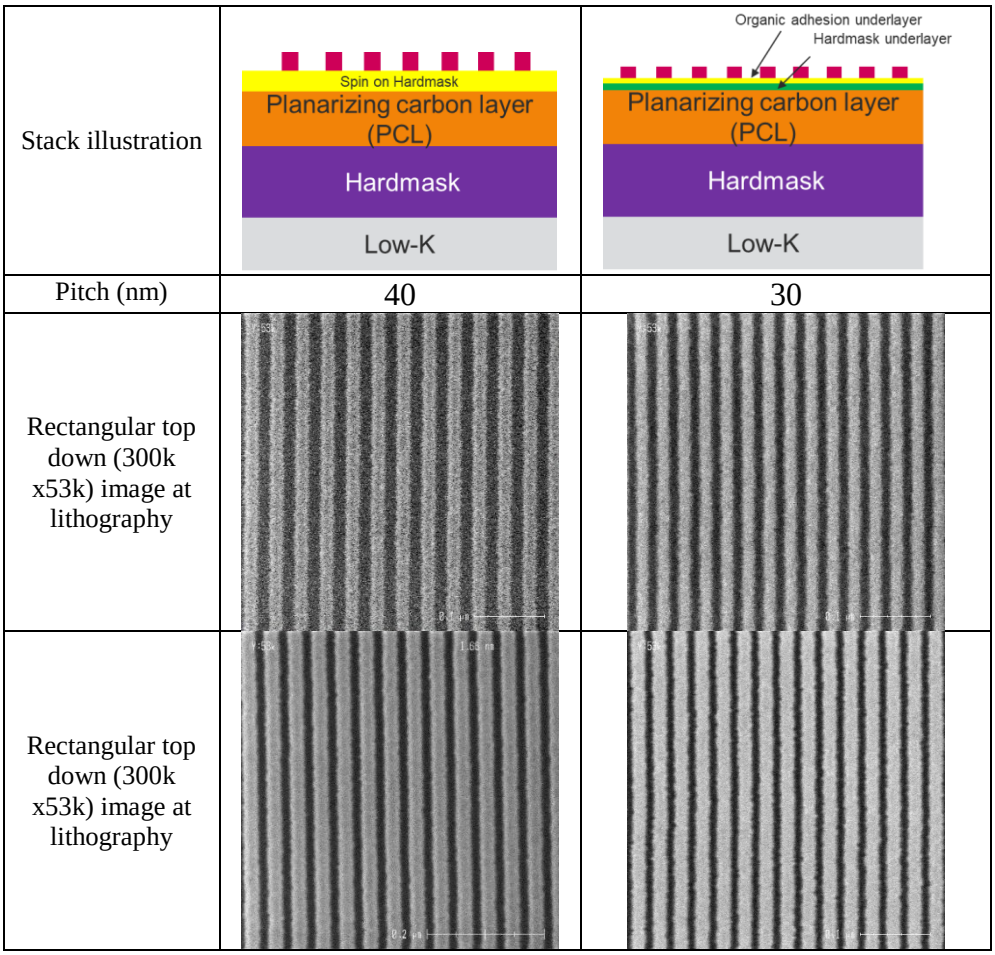


Figure 22: Stack illustration and top down CD SEM images after lithography and hard mask etch.

4.2 Roughness analysis

At 40nm pitch, the unbiased PSD of the Line Edge Roughness and Line Width Roughness shows a typical very clear smoothing after etch in the mid to high frequency region. A 15% reduction of LER and 22% of LWR has been measured. The difference between biased and unbiased value was in this case much larger

when measuring the patterns after lithography which can be explained by the low signal to noise ratio of the images.

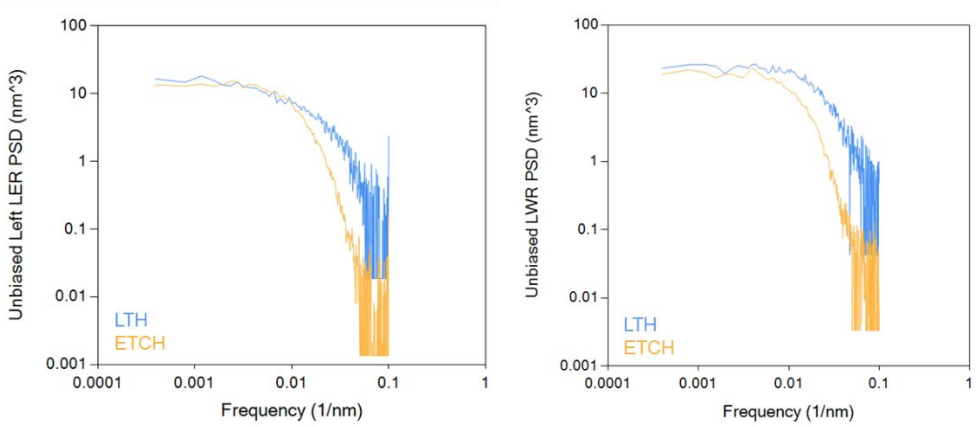


Figure 23: Unbiased PSD of Left-LER and LWR for 40nm pitch EUV lithography.

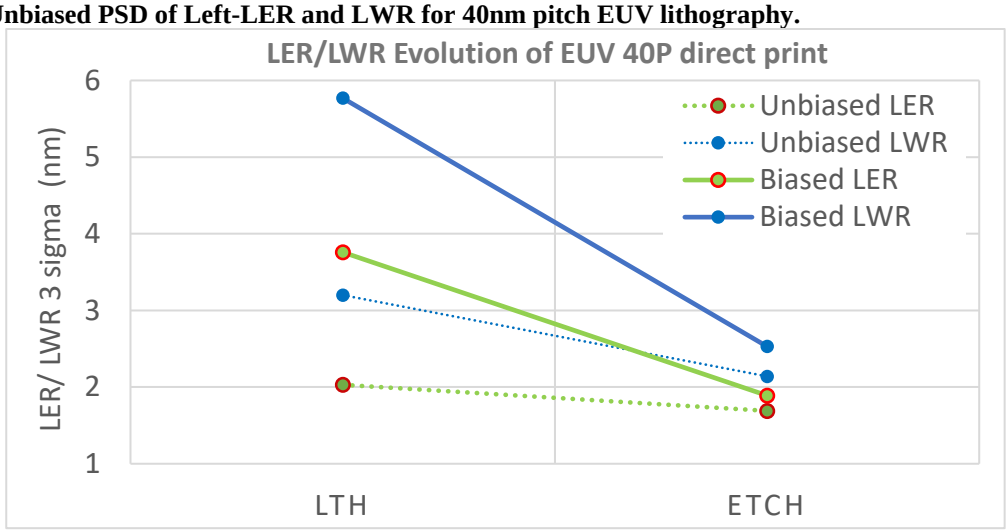


Figure 24: Biased and unbiased LER and LWR (3 sigma) value for EUV 30nm pitch direct print.

However, for 30nm pitch EUV direct print, the PSDs of Figure 25 show an increase in LER and LWR after etch. The high frequency region is still reduced after etch but a degradation occurs in the low to mid frequency area which can be the result of an aspect ratio driven roughness. In order to decrease the low frequency region, the stack would have to be optimized (material type as well as height of each layer). In a similar way, the 30nm pitch shows the most important delta between biased and unbiased value observed at lithography.

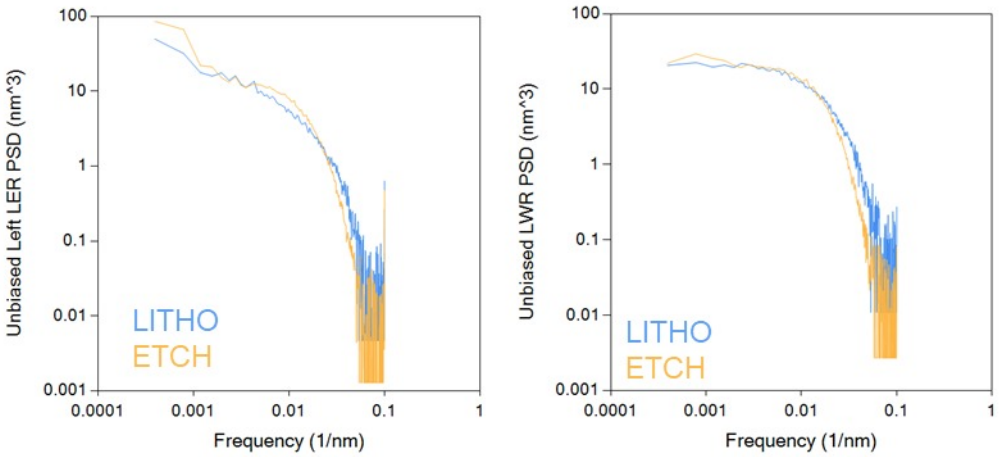


Figure 25: Unbiased PSD of Left-LER and LWR for 30nm pitch EUV lithography.

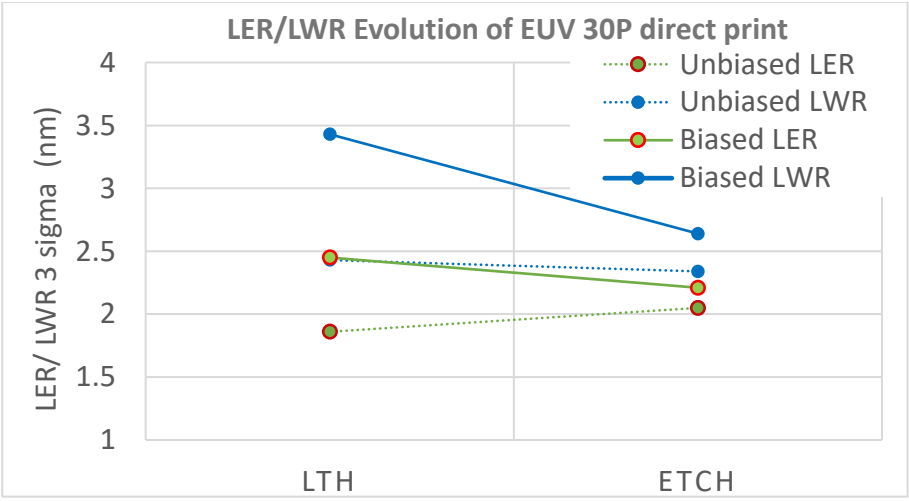


Figure 26: Biased and unbiased LER and LWR (3 sigma) value for EUV 30nm pitch direct print.

5. COMPARISON OF VARIOUS PATTERNING SCHEMES AT EQUIVALENT PITCH AFTER FINAL PATTERN TRANSFER

After studying the roughness evolution of each steps required to define the final structure, we can compare the performance of the different integration schemes to reach a certain pitch. In this section, we will only focus on the roughness of the final patterns.

5.1 40nm pitch patterning technique comparison

First, we compared the two different methods to form a 40nm pitch. As expected, in Figure 27 we observe that the final LWR is much lower for the SADP option due to the correlated edges. The Space Width Roughness (SWR), however, is lower for the EUV direct print, which can be directly explained by the lower LER of this option. We believe that the low frequency LER of the immersion SADP flow can be further reduced

under additional optimization efforts. Nonetheless, the biggest limitation of this integration remains the need for an aggressive mandrel trimming that can cause wiggling due to high aspect ratio.

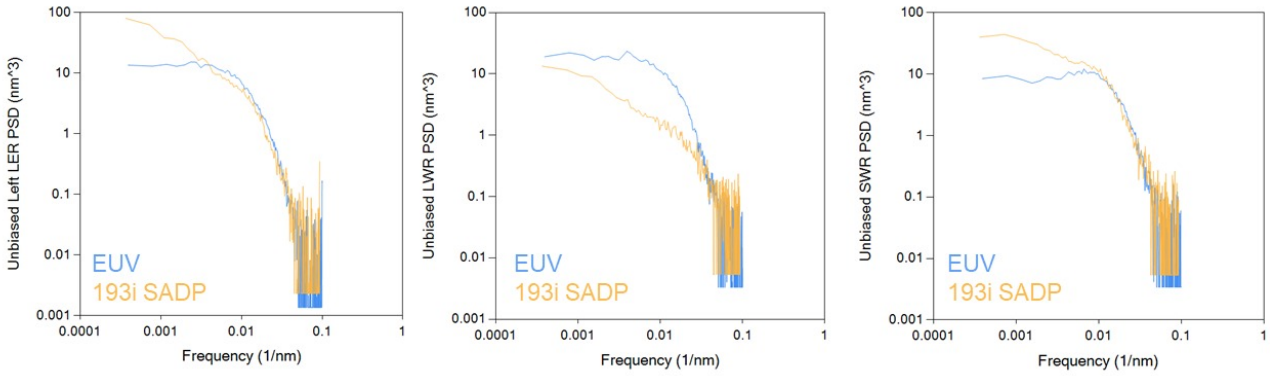


Figure 27: Unbiased PSD of Left-LER, LWR and SWR at 40nm pitch printed with EUV lithography and 193i SADP.

5.2 30 and 28nm pitch patterning technique comparison

In this final section, we are comparing 3 different methods: EUV direct print for 30nm pitch, EUV lithography at 58nm pitch combined with SADP, and finally the SAQP used to reach 30nm pitch. The unbiased PSD of LER on Figure 28 shows no clear differentiation of any method, a slight advantage being given to the SAQP scheme. For the LWR, both self-aligned options (SADP and SAQP) have much reduced roughness, due to left and right edge correlation. Smallest SWR is observed on the SAQP flow and can be explained by the fact that some of those spaces have left and right side correlation (coming from the spacer 1 transferred as the 2nd mandrel).

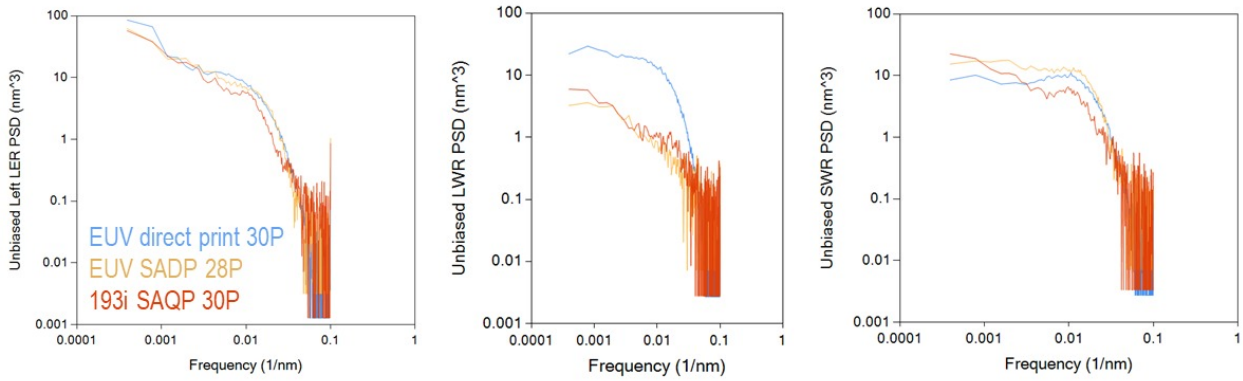


Figure 28: Unbiased PSD of Left-LER, LWR and SWR of 30nm pitch line and space printed with EUV lithography, 28nm SADP EUV and 30nm 193i SAQP.

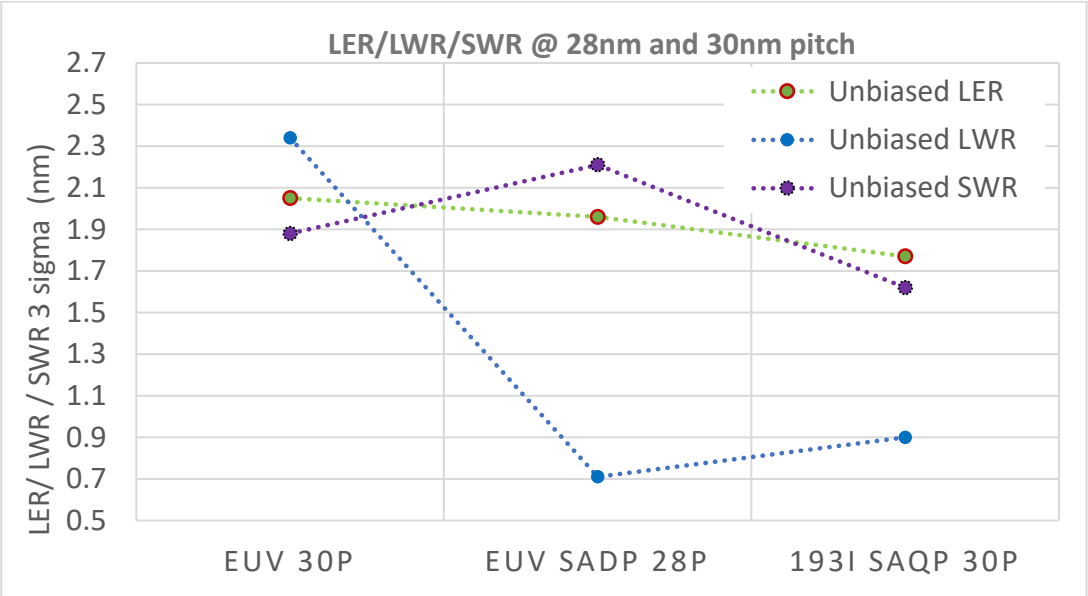


Figure 29: unbiased LER, LWR and SWR (3 sigma) value for 28 and 30nm pitch.

6. CONCLUSION AND OUTLOOK ON EUV LINE AND SPACE

The first generation of EUV patterning for line and space at 20nm half pitch is competitive in terms of LER and SWR. The second node EUV line and space shows different etch impact to PSD and indicates that stack optimization is needed as seen from PSD(0) increase and specific frequency "bump", while high frequency is still rectified. Multipatterning SAQP is still the front-runner approach as it meets both LER and SWR performance targets at 30nm pitch. EUV with SADP for sub 30nm pitch and below can be attractive but needs further LER improvement especially in low frequency region.

Roughness unbiased PSD analysis is a powerful tool to drive process improvement through systematic stack optimization to drive down low frequency increase seen at these aspect ratios.

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