Modeling Edge Placement Error Performance of EUV and DSA Multipatterning Processes

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ABSTRACT

Background: Patterning of very tight pitches suffers from stochastic variations that can impact yield. Different patterning processes with lower stochastic variations are preferred when those lower variations have a quantifiable benefit in terms of device yield or performance.
Aim: Here two different process flows, a traditional EUV patterning flow and one involving directed self-assembly (DSA) rectification, will be compared to determine the differences expected in device failure rates, with the failure mechanism being the shorting of a via hole to the wrong feature.
Approach: These device failure rates will be based on a rigorous edge placement error (EPE) model taking stochastic variations into account, leading to predictions of device failure and the definition of an overlay process window (OPW): the range of overlay errors that keeps the device failure rate above a minimum specified value.
Results: For the patterning of 18 nm pitch line/space patterns contacted with 12 nm wide vias, the EUV process flow produces a 2.5 nm OPW, while the DSA rectification process expands that OPW significantly to 4.0 nm.
Conclusions: Using a rigorous EPE modeling approach fed by accurate stochastics measurements, the significant benefits of the DSA rectification process have been quantified.

Keywords: overlay, edge placement error, EPE, stochastics, directed self-assembly, DSA

1. INTRODUCTION

An important geometry in advanced semiconductor device manufacture is the overlay of a contact/via over a line (or alternatively, the overlay of a line over a via). Electrical device connectivity is achieved when there is sufficient area overlap between the contact hole and the line. Patterning errors, such as overlay errors between these two layers plus local and global variations in the pattern sizes and positions, lead to less-than-ideal area overlap. Further, the need for high density in device designs requires very tight pitches for the lines. These same patterning errors can lead to a contact meant to connect to one line inadvertently touching a neighboring line. Thus, patterning errors, including overlay and stochastics errors, could lead to either electrical opens or shorts. Using a larger target via size reduces the incidence of opens (incomplete contact), but increases the possibility of a short (contact with a neighboring line), and vice versa for a smaller via size. Thus, there is a desire to optimize the design for maximum yield, and for understanding the impact of various process choices on that yield.

In previous work, an approach for rigorously incorporating stochastic variations into overlay and edge placement error (EPE) evaluations and yield predictions was developed.[1] The basic steps in the method are:

1. Write down geometric equations for the problem (involving the overlapping of two patterning layers). Find an equation for the quantity of interest (typically the distance between two edges from the two layers) based on the geometry. This is interpreted as the mean behavior of the process.
2. Take the variance of this equation. This is interpreted as the variance in the parameter of interest as a function of the means and variances of the other geometric terms.
3. Find the stochastic contributors to each term in the variance equation and relate each to a measurable quantity.
4. Define the failure probability (assume a Gaussian distribution, for example). This generally means integrating the probability distribution of the parameter of interest (with mean and variance as defined in the previous steps) with failure defined as a range of values for the parameter of interest.

This method can be applied to a wide variety of patterning problems, and here it will be applied to the contact of a via to a line.

This study will compare two process flows for creating 21 nm pitch and 18 nm pitch lines and spaces. Both processes are based on the extreme ultraviolet (EUV) lithography definition of lines and spaces at twice the pitch followed by a standard self-aligned double patterning (SADP) to divide the pitch by two. The first flow, labeled "EUV", is a standard SADP process flow: the core or backbone pattern (42 or 36 nm pitch) is defined by EUV single patterning, followed by SADP. The second flow, labeled "DSA", changes the backbone patterning to use DSA rectification. The backbone EUV single patterning is carried out at 60% lower dose, resulting in rougher features. DSA is then used to rectify these patterns, creating a smoother and more controlled set of lines and spaces at the same pitch (42 nm or 36 nm).[2] SADP is carried out in the same manner as the with the EUV process flow. Figure 1 illustrates these two process flows.

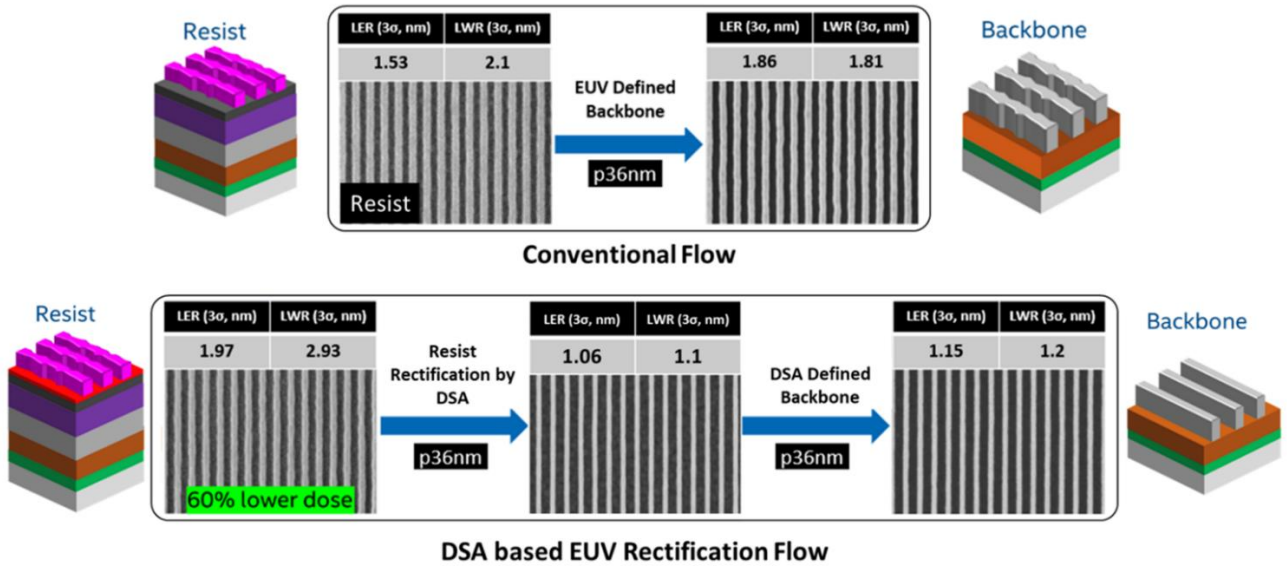


Figure 1. Comparison of the "EUV" conventional flow to produce 18 nm lines and spaces (top) to a "DSA" flow involving DSA rectification of the backbone pattern before SADP (bottom).

For each of these two flows, metal lines are formed in the spaces of the final line/space pattern. The same via patterning step is used to make contact with the resulting metal lines. The goal of this study is to compare the yield impact of these two process flows for both 21 nm pitch and 18 nm pitch metal line connections. Here, only the failure mechanism of a via shorting with a neighboring line will be investigated (leaving the complementary failure mechanism of an incomplete via connection to future work).

2. EDGE PLACEMENT ERROR MODEL

The geometry of contacting a metal line is shown in Figure 2. The two distances of interest are CD_3 and CD_4, the distance from the one edge of the via to one edge of the neighboring line. Due to symmetry, working through the geometry and mathematics of one of these distances (CD_3) is sufficient. The first step in our analysis is a simple geometric interpretation of the distances, without considering process or stochastic variations.

$$CD_3 = Pitch - \frac{CD_{via}}{2} - \frac{CD_{line}}{2} + OVL \qquad (1)$$

where $Pitch$ is the designed x-direction distance between the center of the via and the center of a neighboring line, CD_{via} is the nominal width of the bottom of the via (in the x-direction), CD_{line} is the nominal width of the metal line, and OVL

is the mean x-direction overlay error between the two layers. The equation for CD_4 would simply change the sign of the OVL term.

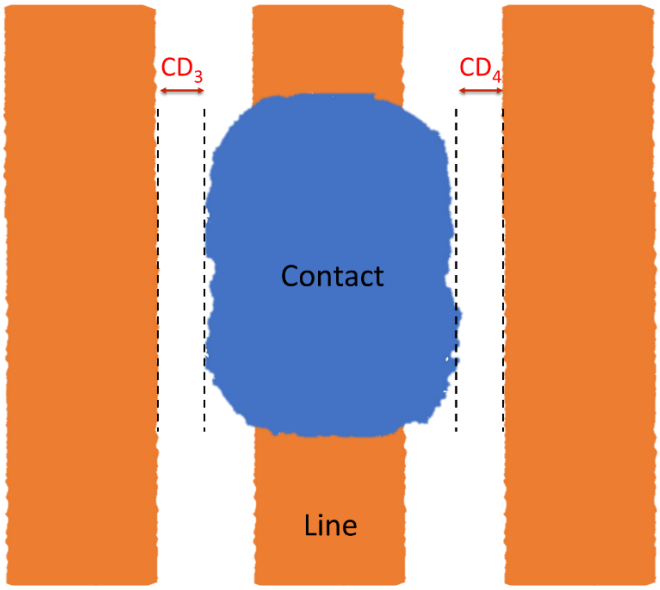


Figure 2. Geometry of contact/via landing over a metal line. The edge-to-edge distances CD_3 and CD_4 will be used to define the probability of the via shorting to a neighboring line.

Taking the variance of this equation (and allowing any variation in the $Pitch$ term to be considered a variation in OVL),

$$\sigma_{CD_3}^2 = \frac{1}{4}\left(\sigma_{CD_{via}}^2 + \sigma_{CD_{line}}^2\right) + \sigma_{OVL}^2 \tag{2}$$

Note that $\sigma_{CD_{via}}$ and $\sigma_{CD_{line}}$ are the combined local CD uniformities (LCDU) and global CD uniformities (GCDU) of the via and line, respectively. The overlay variance term can be broken down into components using

$$\sigma_{OVL}^2 = \sigma_{Res}^2 + \sigma_{LPPE_{via}}^2 + \sigma_{LPPE_{line}}^2 \tag{3}$$

where LPPE represents the local pattern placement error of the line or via and σ_{Res} is the unmodeled residuals of the measured overlay error. An alternate formulation is to combine LCDU and LPPE into a local edge placement error (LEPE). As will be described in the next section, it is possible to measure LEPE directly for the features in each layer. This results in an alternate expression for the variance in CD_3.

$$\sigma_{CD_3}^2 = \sigma_{GCDU_{via}}^2 + \sigma_{GCDU_{line}}^2 + \sigma_{LEPE_{via}}^2 + \sigma_{LEPE_{line}}^2 + \sigma_{Res}^2 \tag{4}$$

It is important to note that $\sigma_{LCDU_{line}}$, $\sigma_{LPPE_{line}}$, and $\sigma_{LEPE_{line}}$ are not measured over the entire length of a line, but over a segment length chosen for its device relevance. For a very long line, each of these three variations tend towards zero. But if the line is cut up into many smaller segments, the width, center, and edge position of each segment can be used to determine LCDU, LPPE, and LEPE. Here, the segment length of relevance relates to the overlap of the via with the line. Since the failure mechanism of interest here is the touching of a neighboring line with the via, line variation over length equal to some fraction of the via height is most important (see Figure 3). In this study, 50% of the via height will be used (which is a segment length of 8 nm).

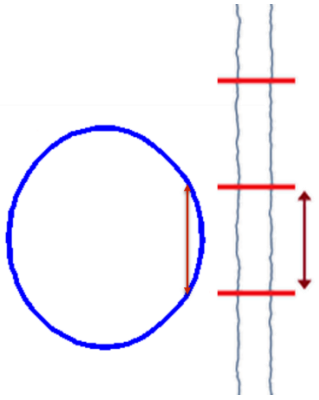


Figure 3. The segment length to be used for the measurement of LCDU, LPPE, and LEPE of the line is chosen to be a fraction of the via height (in this case, 50% of the via height is shown). The via contour shown is the mean contour of all the vias measured for this study.

The final step in our EPE modeling approach is to define a failure mechanism, then determine the rate of failure as the probability that this failure mechanism will occur. Here, failure will be $CD_3 < 0$ or $CD_4 < 0$. Assuming that each of these distances follows a Gaussian distribution with mean given by equation (1) and variance given by either equations (2) and (3) or equation (4), the probability of failure becomes

$$Probability(CD_3 < 0) \approx \frac{\sigma}{\sqrt{2\pi}\mu} e^{-\frac{\mu^2}{2\sigma^2}} \tag{5}$$

where the exact error function expression has been approximated as an exponential for the case of low failure probability.[1] It is useful to note that this failure probability is only a function of the ratio σ_{CD_3}/μ_{CD_3}.

One use for the calculated failure rate is to create an overlay process window (OPW).[1] The failure rate for both CD_3 and CD_4 are added together and then plotted as a function of OVL, the x-direction overlay error (Figure 4). By defining a maximum acceptable failure rate (for example, 1X10^{-10}, or 0.1 ppb), the range of overlay that keeps the failure rate below this threshold can be determined and is called the OPW.

Measurement uncertainties propagate from individual measurement terms (such as $\sigma_{LEPE_{line}}$) to the calculated term of interest (σ_{CD_3}), and finally to the overlay process window result. The standard error $SE(\sigma_{CD_3})$ is approximately, for small errors, using

$$\begin{aligned}\left(SE(\sigma_{CD_3})\sigma_{CD_3}\right)^2 \approx (SE(\sigma_{Res})\sigma_{Res})^2 + \left(SE(\sigma_{GCDU_{via}})\sigma_{GCDU_{via}}\right)^2 + \left(SE(\sigma_{LEPE_{via}})\sigma_{LEPE_{via}}\right)^2 \\ +\left(SE(\sigma_{GCDU_{line}})\sigma_{GCDU_{line}}\right)^2 + \left(SE(\sigma_{LEPE_{line}})\sigma_{LEPE_{line}}\right)^2\end{aligned} \tag{6}$$

The standard error of the OPW becomes

$$SE(OPW) = 2(\mu_{CD_3}/\sigma_{CD_3})SE(\sigma_{CD_3}) \tag{7}$$

where μ_{CD_3}/σ_{CD_3} is the value at the maximum allowed failure rate and is thus determine solely by that maximum allowed failure rate. For a failure rate threshold of 0.1 ppb, $2(\mu_{CD_3}/\sigma_{CD_3}) = 12.7$. To have good confidence in the calculated OPW values, a metrology approach must be used that keeps $SE(\sigma_{CD_3})$ small due to thus multiplier of 12.7.

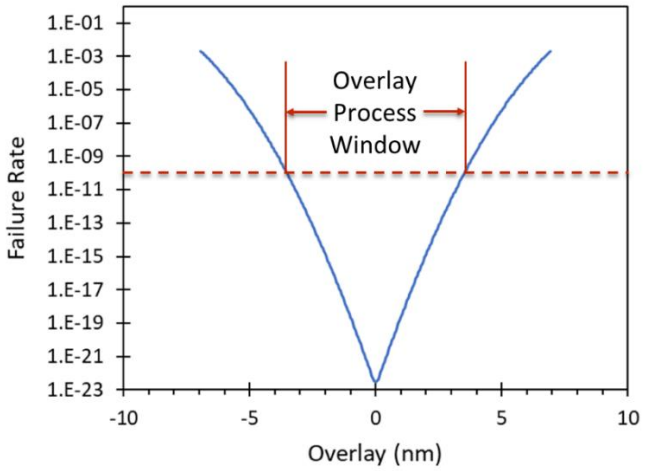


Figure 4. The overlay process window (OPW) is defined by applying a maximum acceptable failure rate (0.1 ppb is shown here) to a calculation of failure rate versus overlay error. The range of overlay errors that keeps the failure rate below this threshold is called the OPW.

3. MEASUREMENT OF MODEL TERMS

An advantage of the EPE modeling approach used here is that all terms in the model are measurable. In particular, the LCDU, LPPE, and LEPE terms can be measured with SEM images for each layer individually (line/space and via), and the mean and residual overlay error between the layers are measured using the standard plan of record approach (for example, optical scribe-line measurements). Figure 5 provides details of the SEM-based metrology setup for the line/space and via layers. Metrology results are presented in Table I, where MetroLER v4.2.0 (from Fractilia) was used for all measurements. Unbiased values of LCDU, LPPE, and LEPE are given. Note that the stochastic measurements for the spaces are used since these spaces will be metalized and contacted with the vias. For the vias, the results for the 21 nm pitch process are presented, with a mean X CD for the via at the point of contact with the metal line determined to be 13 nm. For the 18 nm pitch the via size is scaled to 12 nm, though the stochastic variation results are assumed to be the same. Edge placement errors are measured for both the left edge and the right edge, but only the maximum of these two is shown in the table (since it is the maximum of the two edges that will impact the failure rate).

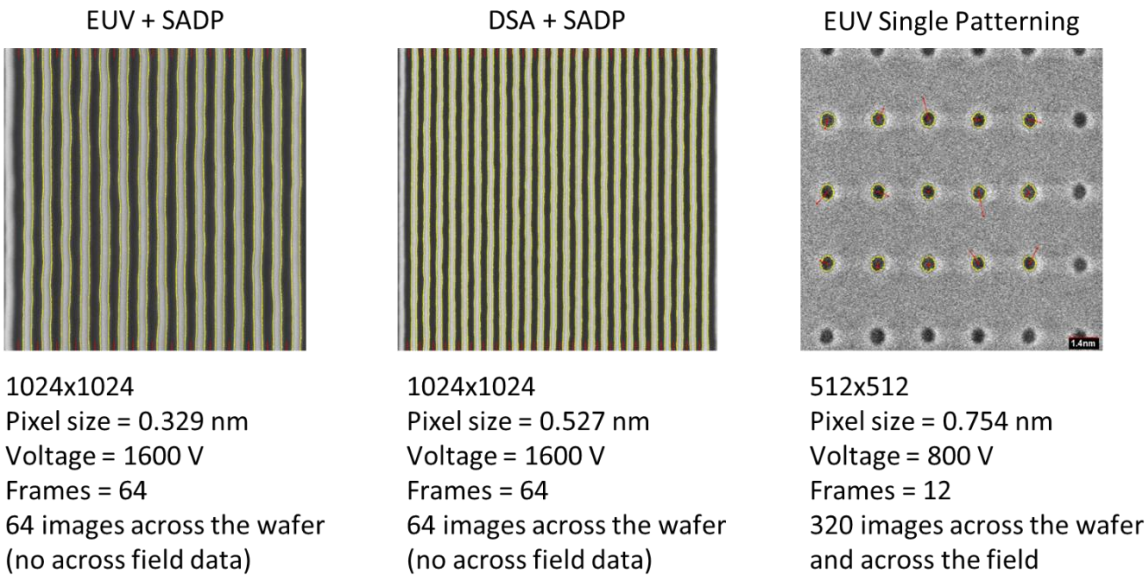


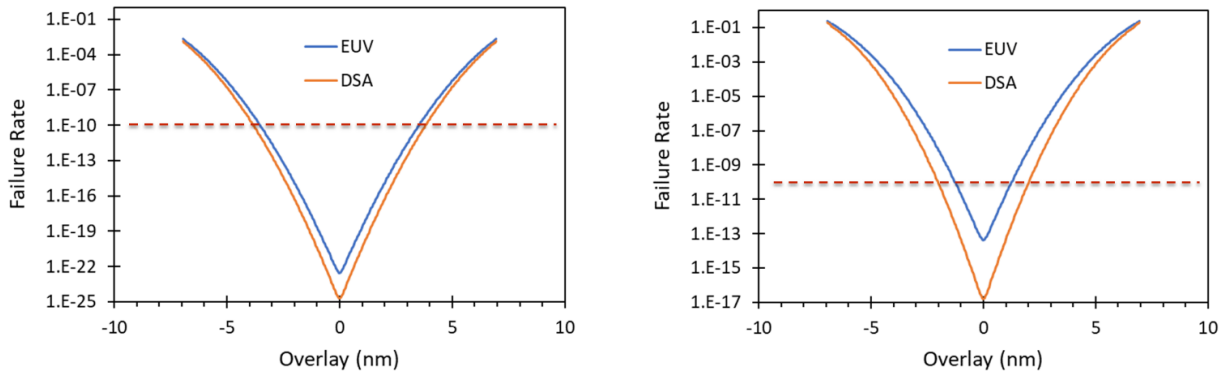
Figure 5. Details of the SEM-based metrology for each layer.

*Table I. Metrology results, measured with MetroLER. GCDU, LCDU, LPPE, and LEPE values are 3σ. LCDU, LPPE, and LEPE reported values are unbiased. Uncertainty estimates are ± 2*Standard Error. For LEPE, the worst of right or left edge is used.*

Parameter	Mean (nm)	GCDU (nm)	LCDU (nm)	LPPE (nm)	LEPE (nm)
21 nm pitch, EUV Space CD	11.7	0.33 ± 0.06	2.09 ± 0.02	1.161 ± 0.008	1.58 ± 0.01
21 nm pitch, DSA Space CD	11.6	0.67 ± 0.12	1.157 ± 0.007	1.071 ± 0.005	1.272 ± 0.006
18 nm pitch, EUV Space CD	9.5	0.38 ± 0.06	2.89 ± 0.02	1.260 ± 0.009	1.91 ± 0.013
18 nm pitch, DSA Space CD	10.4	0.55 ± 0.05	1.43 ± 0.01	0.911 ± 0.006	1.207 ± 0.008
Via X CD	13/12	2.1 ± 0.15	2.03 ± 0.04	1.46 ± 0.03	1.76 ± 0.02

4. RESULTS AND DISCUSSION

The parameter values from Table I can be used in the EPE model. The additional overlay uncertainty term, σ_{Res}, was not measured but was assumed to be 0.5 ± 0.02 nm. For the mean CD values, it was assumed that the differences between the EUV process and the DSA process could be adjusted so that the means would match. Thus, for EPE modeling the mean space CD used for the 21 nm and 18 nm pitches were 11.6 and 10.0 nm, respectively. From the uncertainties in the model terms shown in Table I, the standard error for the calculated σ_{CD_3} is SE(σ_{CD_3}) ≈ 0.008 nm. The resulting failure rates and overlay process windows are shown in Figure 6.



(a) (b)

Figure 6. Failure rates calculated based on the data in Table I for (a) 21 nm pitch case, and (b) 18 nm pitch case.

From these results, the Overlay Process Window (OPW) for 21 nm pitch and the EUV process is 6.9 ± 0.2 nm, and for the DSA is 7.5 ± 0.2 nm. The improvement in overlay process window by using the DSA rectification process for the 21 nm pitch case is modest but statistically significant. For the 18 nm pitch case, the EUV process has a the smaller OPW of 2.5 ± 0.2 nm, while the DSA process has a much larger OPW of 4.0 ± 0.2 nm. Clearly, the lower stochastics of the 18 nm pitch DSA-rectified patterns results in a significant advantage in terms of the overlay process window.

The EPE model can also be used for parametric studies. For example, how does a change in the mean via CD affect the failure rate? The model confirms intuition: a 1 nm increase in the mean via CD produces a 1 nm decrease in the overlay process window. Another parameter needed in analyzing the measurement data is the segment length used to determine the EUV and DSA space stochastic terms (such as LEPE). Choosing 8 nm (half of the via height) is reasonable, but somewhat arbitrary. Choosing 4 nm instead allows for a new measurement of LEPE and prediction of the overlay process window. For the 18 nm pitch case, the result is a 1% decrease in the DSA OPW value, and a 2% decrease in the EUV OPW. Since these changes in OPW are significantly smaller than the OPW error bars, we conclude that segment lengths in this range are adequate for proper OPW analysis. The reason has to do with the correlation length of the LER. For the 18 nm pitch EUV line/space pattern, the LER correlation length is 10 nm while for the DSA process it is 8 nm. Since the statistical behavior of an edge over a distance less than the correlation length is highly correlated, choosing segment lengths less than the correlation length produce similar statical variation.

In this study, global variations in the CD of both the spaces and the vias were considered random variations and added as terms in the expression for σ_{CD_3}. An alternate approach is to consider at least some of the global variation to be a systematic error that simply offsets the mean value of the space and via CDs. For example, a measurement of via CD across the wafer or across the chip could be thought of as shifts in mean via CD, allowing a calculation of the OPW across the wafer/chip. Coupling this systematic variation with across-wafer/chip variations in space CD and mean overlay would produce a mapping of expected die yield across the wafer.

Another variation in the analysis would be to measure the line/space patterns as an SADP data set, where two statistical populations of lines and spaces are separated and their stochastics analyzed for each population separately. Then separate overlay process windows could be established for each population, and the sum of the two failure rates can be analyzed using a minimum failure rate specification of 0.2 ppb for the total. In this case, the EUV processes exhibited some pitch walking: the line CD was the same between the two populations but the space CD differed by 0.66 nm. For the DSA process, the line CD varied between the two populations by 0.27 nm, and the space CD by 0.08 nm. This pitch walking (or CD imbalance) will have a direct and negative impact on the overlay process window. Ignoring the pitch walking, the differences in the stochastics behaviors of the two populations did not have an appreciable impact of the OPW. Thus, the key difference between the EUV and DSA processes with respect to the SADP step will be how well each process can be optimized for minimum CD imbalance between populations. For the failure mechanism studied here (a via shorting with a neighboring line), it is the space CD imbalance that matters.

5. CONCLUSIONS

DSA rectification offers several advantages over the standard EUV-only process for making the backbone pattern of SADP formation of 21 nm and 18 nm pitch line/space patterns. For DSA rectification, the EUV exposure dose can be reduced by 60% while still achieving well controlled results. And the results after SADP show that the DSA process flow produces features with lower stochastic variation (lower LER and LWR).

Despite these clear advantages, it can still be difficult to quantify the benefits of such lower stochastic variation in terms that are more easily correlated to monetary value. The EPE modeling approach used here, with its calculation of failure rates as a function of known process variations such as overlay error, can be used to evaluate the benefits of the DSA process flow over the traditional EUV process flow more concretely. In this study, a modest but statistically significant improvement in the overlay process window was seen for the patterning of the 21 nm pitch design rule devices. Note that a rigorous analysis of edge placement errors leading to an assessment of the overlay process window is much more useful when coupled with a rigorous analysis of measurement uncertainty propagation in order to determine if the resulting difference is statistically significant.

For the 18 nm pitch design rule the advantage of the DSA process flow is quite significant, with an overlay process window (4.0 nm) that is 60% larger than for the EUV process flow (2.5 nm). If, for example, overlay errors of the via with respect to the line/space pattern are expected to be in the range of ±1.5 nm, the EUV process flow could be expected to be very low yielding while the DSA process flow would be high yielding (with respect to the failure mechanism studied here).

The OPW study presented here could be made more complete by adding the additional failure mechanism of poor overlap of the via with the intended line to be contacted. While we expect to complete this future work, the conclusions will only reinforce the benefits of the DSA rectification process over the conventional EUV process. Including this failure mechanism, however, would allow for the optimization of the target via CD as the value which produces the largest overlay process window.

6. ACKNOWLEDGEMENTS

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