Spatial Frequency Analysis of LER and LWR to Tune SADP Process

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INTRODUCTION

Continued scaling of memory and logic devices poses many challenges that cannot be solved through advanced lithography techniques alone. Multi-patterning techniques have enabled extremely small line widths through SAxP and LEx, but there are still many challenges that limit scaling. The largest variation in a typical SADP process is feature roughness, defined as LER (line edge roughness), LWR (line width roughness), and SWR (space width roughness). Roughness is rapidly becoming the key scaling limiter and addressing this with deposition and etch provides an opportunity for materials-enabled solutions to facilitate device scaling [1].

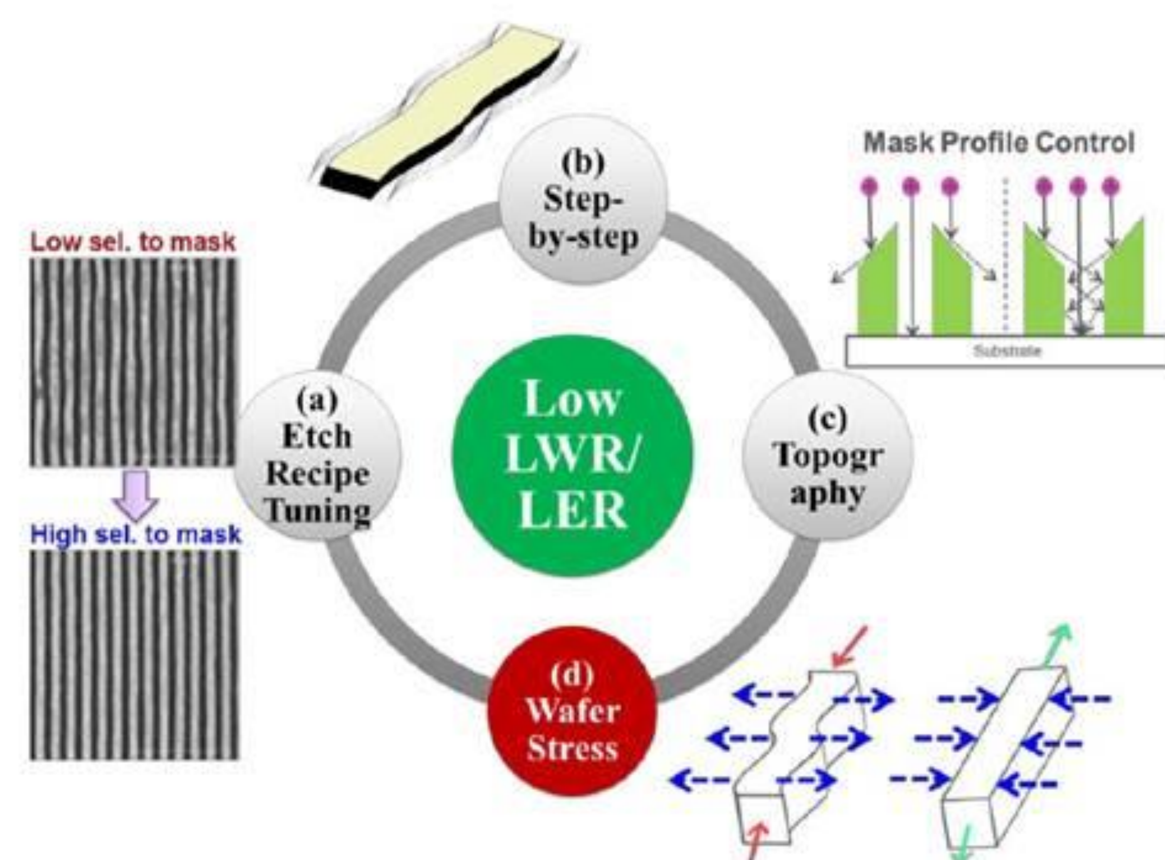


Fig. 1 Potential line roughness performance improvement solutions on SAxP flow [1].

METHODS

In the SADP process, controlling roughness of the final spacer is the key challenge to achieve good pattern transfer. It's therefore critical to understand where roughness originates throughout the process flow. Using unbiased power spectral densities, thorough analysis of different frequency ranges (Low, Middle, High) per process step were quantified [2]. In this way, it was possible to observe that the deposition step introduces Low to Middle frequency LWR.

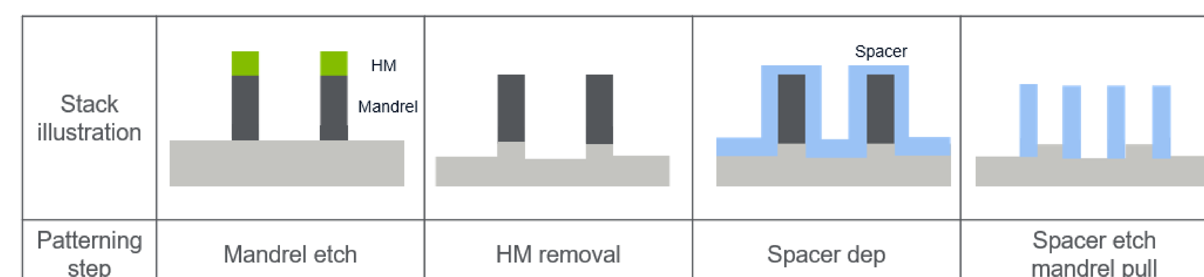


Fig. 2 SADP stack and process flow illustration.

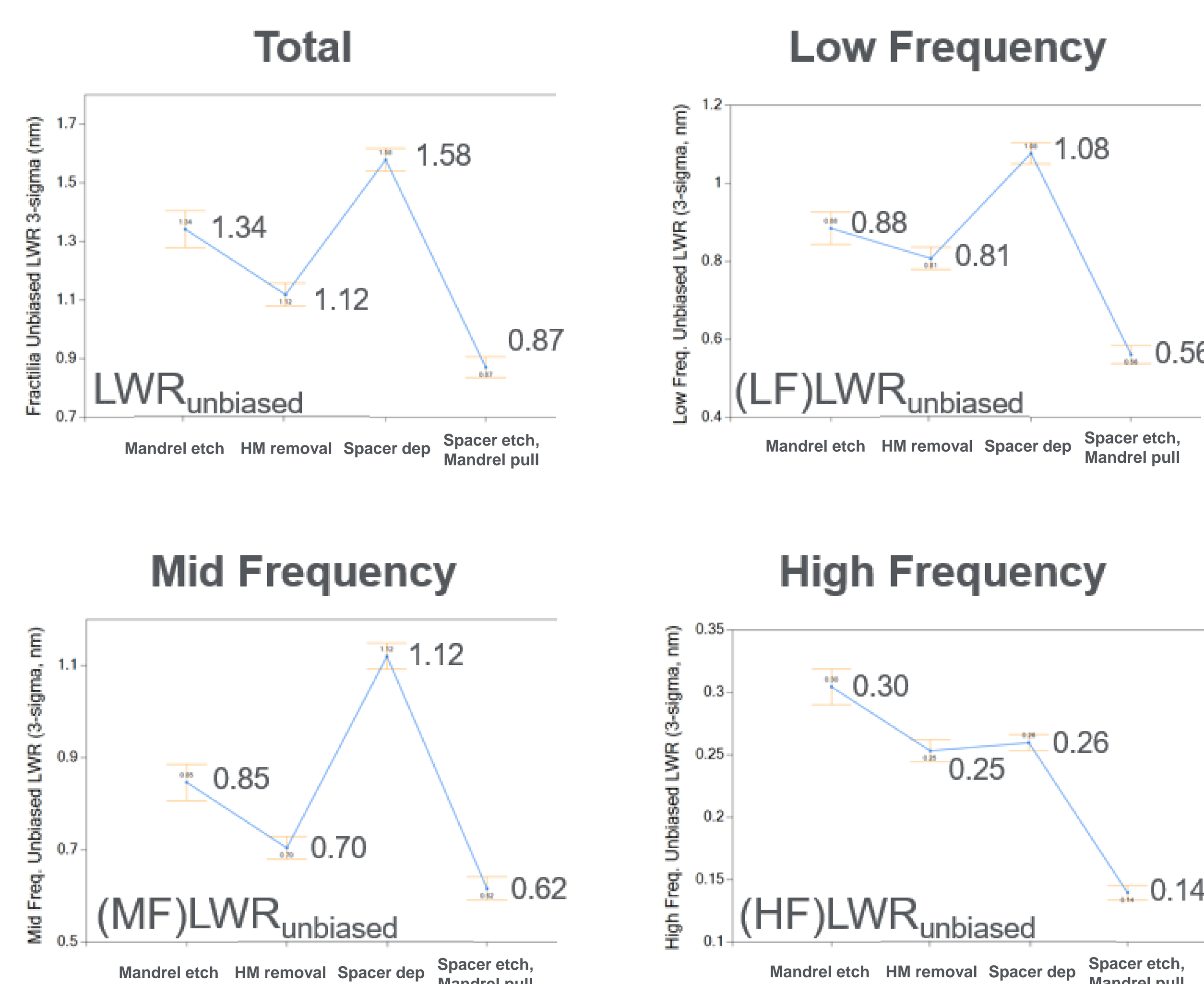
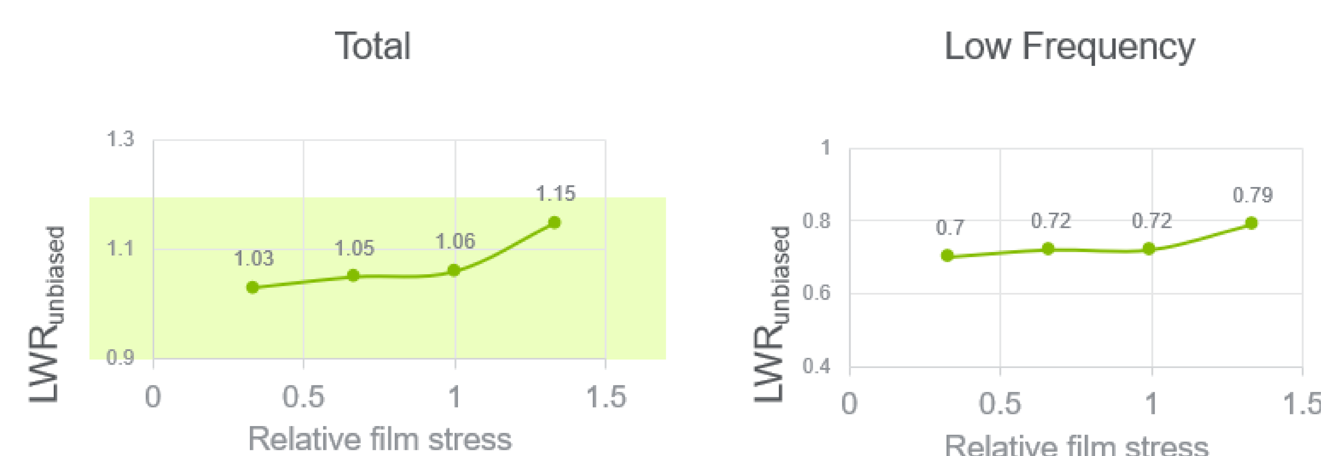


Fig. 3 Deposition step introduces Low to Middle frequency LWR. Length for low frequencies: 50nm. Length for high frequencies: 10nm.

RESULTS

Process co-optimization is key to controlling final CD spacer roughness. Tweaking thin film stress during spacer deposition enables further LWR reduction post etch. Tuning the etch power condition has been shown to reduce line wiggling (responsible for Low frequency LER), while adjusting gas flow can minimize residue by mitigating re-deposition (thus improving Middle frequency LER).



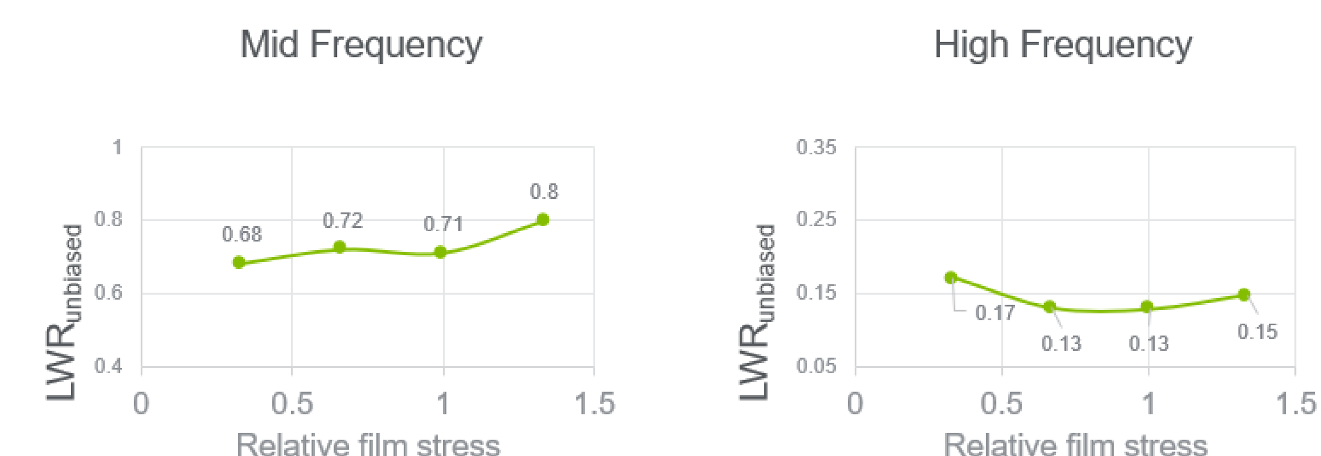
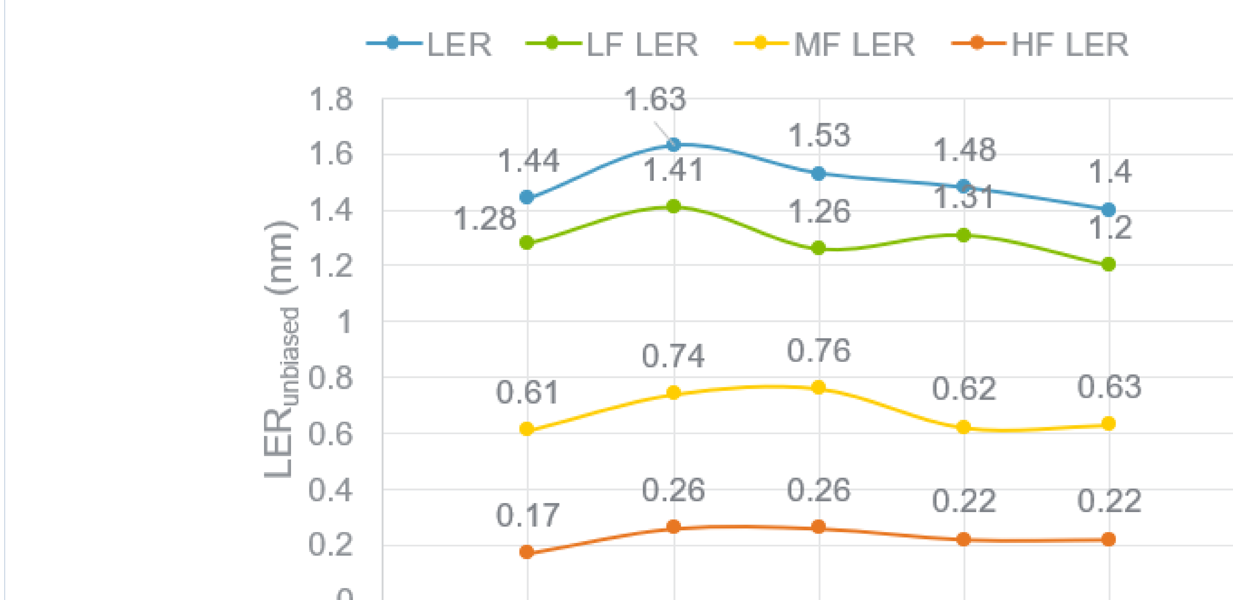


Fig. 4 Lowering thin film stress levels during deposition enables further spacer LWR reduction after the etch step.



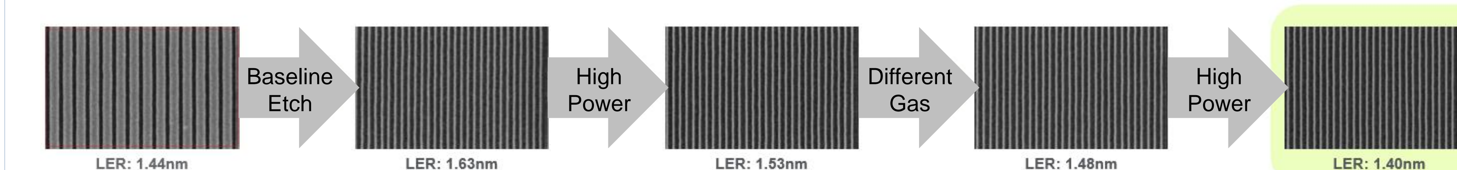


Fig. 5 Low to Middle frequency LER can be minimized through proper etch step tuning.

CONCLUSIONS

Analysis of roughness frequency ranges per SADP process step aids co-optimization of spacer deposition and etch to rapidly reduce LER and LWR.

REFERENCES

1. Liu, Eric, et al. "Roughness and uniformity improvements on self-aligned quadruple patterning technique for 10nm node and beyond by wafer stress engineering." *SPIE Advanced Lithography*. TEL Technology Center, 2017.
2. Raley, Angelique, et al. "Benchmarking of EUV lithography line/space patterning versus immersion lithography multipatterning schemes at equivalent pitch." *SPIE Advanced Lithography*. TEL Technology Center, 2018